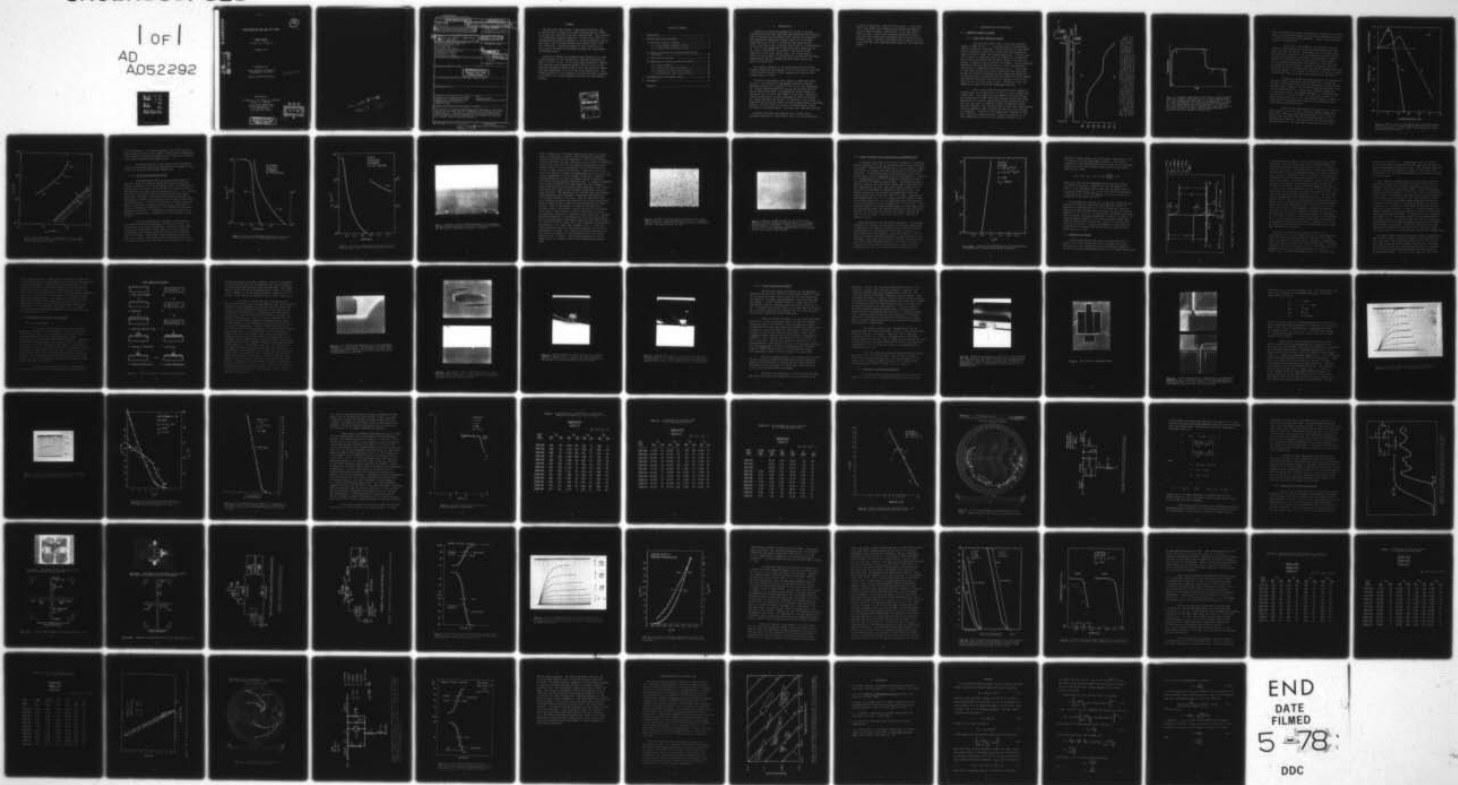


AD-A052 292 VARIAN ASSOCIATES PALO ALTO CALIF CORPORATE SOLID ST--ETC F/6 9/5
HETEROJUNCTION GATE GAAS FET STUDY.(U)
OCT 77 H MORKOC, S G BANDY, R SANKARAN N00173-76-C-0317

UNCLASSIFIED

NL

1 of 1
AD
A052292



AD A 052292

AD No.
DDC FILE COPY

3 Jan. 78

(12)

HETEROJUNCTION GATE GAAs FET STUDY

FINAL REPORT

(76 Aug 23 - 77 Aug 23)

October 1977

Prepared for:

Naval Research Laboratory
Washington, DC 20375

Contract N00173-76-C-0317

532,619

Prepared by:

H. Morkoç, S. G. Bandy, R. Sankaran
and G. A. Antypas

Solid State Laboratory ✓
Varian Associates, Inc.
611 Hansen Way
Palo Alto, CA 94303

DDC
RECEIVED
APR 6 1978
B

DISTRIBUTION STATEMENT A

Approved for public release;
Distribution Unlimited

use code 409910

Corporate Solid State Lab.

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER FINAL REPORT		2. RECIPIENT'S CATALOG NUMBER Final Rept. 23 Aug 76-23 Aug 77
3. TITLE (and Subtitle) Heterojunction Gate GaAs FET Study:		4. TYPE OF REPORT PERIOD COVERED FINAL REPORT (76 AUG 23 - 77 AUG 23)
5. AUTHOR(s) H. Morkoç, S. G. Bandy, R. Sankaran, G. A. Antypas		6. PERFORMING ORG. REPORT NUMBER
9. PERFORMING ORGANIZATION NAME AND ADDRESS Varian Associates, Inc. 611 Hansen Way Palo Alto, CA 94303		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
11. CONTROLLING OFFICE NAME AND ADDRESS DCASMA San Francisco 1250 Bayhill Drive San Bruno, CA 94066		12. REPORT DATE Oct 77
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)		13. NUMBER OF PAGES 75 79 p.
		15. SECURITY CLASS. (of this report) UNCLAS.
		15a. DECLASSIFICATION DOWNGRADING SCHEDULE
16. DISTRIBUTION STATEMENT (of this Report) <div style="border: 1px solid black; padding: 5px; text-align: center;">DISTRIBUTION STATEMENT A Approved for public release; Distribution Unlimited</div>		
17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)		
18. SUPPLEMENTARY NOTES		
19. KEY WORDS (Continue on reverse side if necessary and identify by block number) Normally-off heterojunction FETs Microwave FETs Normally-on heterojunction FETs Subnanosecond logic devices AlGaAs-GaAs heterojunctions Submicron FETs		
20. ABSTRACT (Continue on reverse side if necessary and identify by block number) This project is aimed at developing the technology to fabricate Al _{0.5} Ga _{0.5} As gate GaAs FETs with submicron gate dimensions and to compare the dc, large-signal switching and small-signal microwave performance of both normally-on and normally-off devices with similar Schottky-barrier devices.		

DD FORM 1 JAN 73 1473

EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

409 910

SUMMARY

The microwave small signal, large-signal switching, and dc performances of normally-on (N-ON) and normally-off (N-OFF) $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ gate GaAs FETs have been characterized. The structure is a three-layer sandwich formed by a n-type active layer on a Cr-doped semi-insulating substrate, a p-type Ge-doped $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ gate layer, and a p^+ -type Ge-doped GaAs contact layer on the top of the gate. Selective-etching of the p^+ -GaAs and the p- $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ provides the necessary overhang for self-aligned device fabrication.

Normally-on HJFETs with submicron gate lengths and an associated periphery of 300 microns gave a maximum available gain (MAG) of 9 dB at 8 GHz. On the other hand, normally-off devices with submicron gate dimensions showed a MAG of 9 dB at 2 GHz. Intrinsic propagation delay times of both N-ON and N-OFF HJFETs have been determined to be 20 ps and 40 ps respectively. The contact potential of the heterogate junction has been calculated to be about 1.4 eV, which compares well with the experimental results.

ACCESSION for	
NTIS	White Section <input checked="" type="checkbox"/>
DDC	Buff Section <input type="checkbox"/>
UNANNOUNCED <input type="checkbox"/>	
JUSTIFICATION	
PER FORM 50	
BY	
DISTRIBUTION/AVAILABILITY CODES	
Dist.	Alt. and/or SPECIAL
A	

TABLE OF CONTENTS

1. INTRODUCTION	1
2. INVESTIGATION AND DISCUSSION	3
2.1 Materials Growth of HJFETs	3
2.1.1 Vapor Phase Epitaxial Growth	3
2.1.2 Liquid Phase Epitaxial Growth	9
2.2 Contact Potential of p-AlGaAs/n-GaAs Hetero structures	16
2.3 Fabrication Technique	18
2.4 Experimental Results and Test Procedures	22
2.4.1 Gate Formation	22
2.4.2 Contact Resistivity Studies	29
2.4.3 Normally-On HJFET Device Results	30
2.4.4 Normally-Off HJFET Device Results	48
3. RECOMMENDATIONS FOR FURTHER STUDY	70
4. REFERENCES	72
APPENDIX	73

1. INTRODUCTION

Normally-on (N-ON) and normally-off (N-OFF) $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ heterojunction gate GaAs FETs have been fabricated and characterized as microwave and high-speed logic devices with submicron gate dimensions. The active channel layer with a net donor concentration of 10^{17}cm^{-3} is grown by vapor phase epitaxy (VPE). Then the p-type $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ layer doped to a concentration of 10^{18}cm^{-3} with Ge and the p^+ -type GaAs layer doped with Ge to a level of $5 \times 10^{18}\text{cm}^{-3}$ are grown by LPE following mesa formation on the n-type active layer. The active layer is about 0.13 micron and 0.35 micron thick for N-OFF and N-ON FETs respectively, and the p-AlGaAs and the p^+ -GaAs layers are about 0.5 micron each.

The contact potential of the heterogate using 345-micron diameter diodes has been deduced to be 1.39 eV from C-V data and 1.356 from the forward I-V data, agreeing well with the calculated value of 1.4 eV.

To form the heterogate, the p^+ -GaAs is etched selectively in a pH = 7.05 solution of $\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$ followed by a second selective etching of $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ at 90°C , or in room temperature HF. Further undercutting of the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ provides the overhang of the p^+ -GaAs which is necessary for self-alignment of the source and the drain with respect to the gate. AuGe/Ni/Au contact metallization is then evaporated to form the contacts on n and p-type GaAs and alloyed. In addition, an Au overlay is evaporated on the source, drain, and gate bonding pads to facilitate bonding. The back side of the wafer is thinned down to about 150 microns and plated before it is diced into individual devices.

Normally-on HJFETs with submicron gate lengths and an associated periphery of 300 microns gave a dc transconductance

of about 25 mmhos and a MAG of 9 dB at 8 GHz. On the other hand, N-OFF HJFETs with submicron gate dimensions showed a g_m of 15 mmhos at about a gate bias of +1.0 V and a MAG of 9 dB at 2 GHz. Large-signal switching properties of both N-ON and N-OFF HJFETs have been determined with the aid of a sampling scope. Intrinsic propagation delay times of 20 psec and 40 psec have been observed respectively for N-ON and N-OFF HJFETs.

2. INVESTIGATION AND DISCUSSION

2.1 MATERIALS GROWTH OF HJFETs

2.1.1 Vapor Phase Epitaxial Growth

The vapor epi reactor used to grow active channel layers is shown in Fig. 1. A two-zone roll-on type Marshall furnace is used for this work. The Ga source is at about 828°C and the substrate at about 818°C during the high temperature vapor etch and at about 766°C during deposition. To begin with, the Ga source is saturated with As by bubbling H_2 through the $AsCl_3$ liquid and flowing the (H_2+AsCl_3) mixture over the Ga to produce a complete crust of GaAs on its surface. During subsequent deposition runs the substrate, which is (100)-oriented GaAs, goes through a temperature cycle given in Fig. 2. Since some As loss from the source and crust dissolution must take place during the cooling and heating periods, during any deposition run the Ga source is resaturated with As after the 15-min thermal equilibration by passing 500 cc/min of (H_2+AsCl_3) over it for about 30 min, the $AsCl_3$ being at 20°C. During this time, the substrate is kept at the high temperature position.

Due to crust dissolution during the early stages of resaturation, the Ga source will be only partially covered with a GaAs crust. With some liquid Ga exposed to the gas stream, the calculations of Shaw¹ show that the equilibrium vapor phase composition will contain significantly lower concentrations of HCl , As_4 , As_2 , and Cl_2 compared to when a completely crusted source is exposed. Also the Ga/As ratio in the vapor phase passing into the deposition zone is quite high when the crust coverage is incomplete. Therefore at the temperatures employed in this work, deposition conditions exist around the substrate in the high temperature position with a partially crusted source.

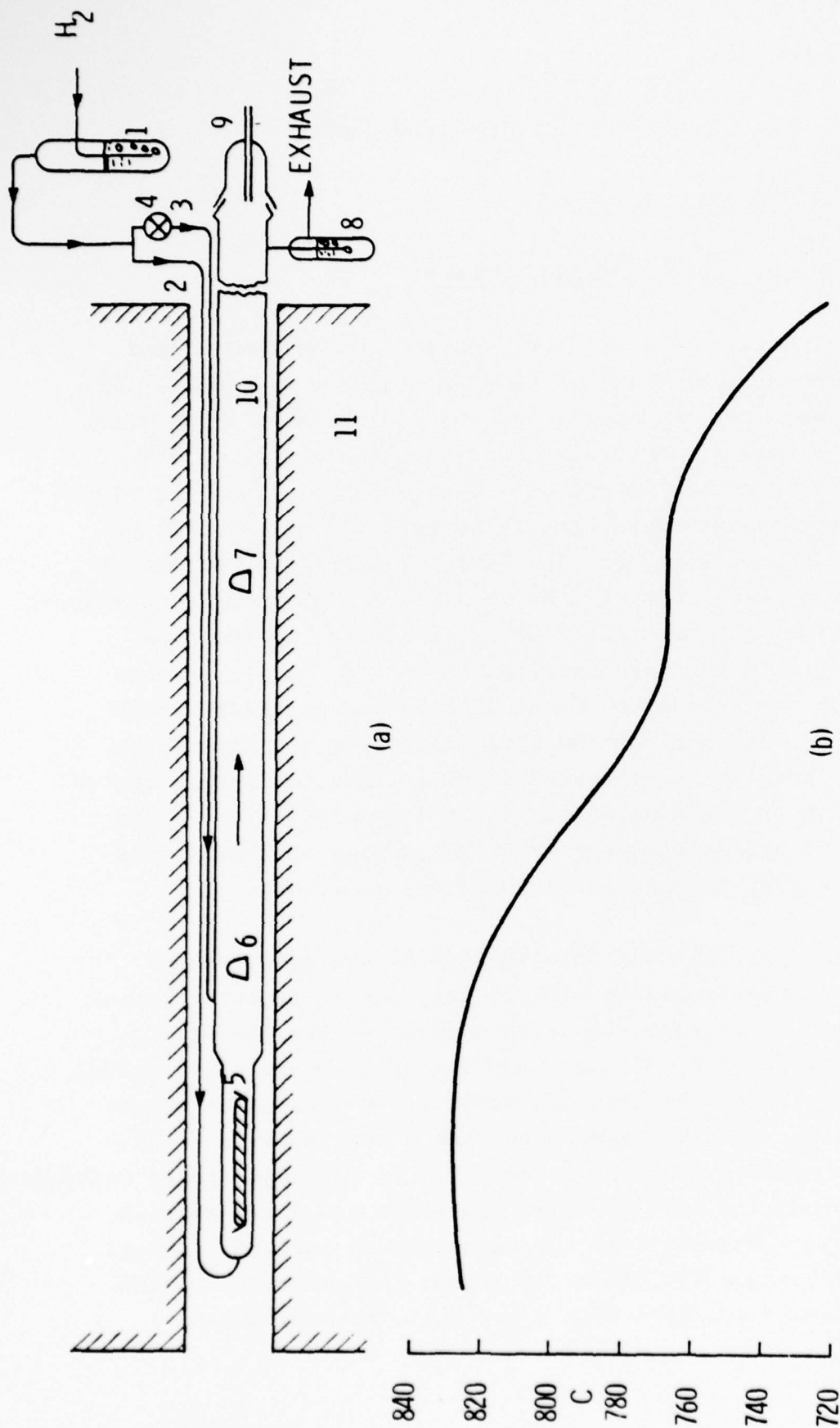


Fig. 1. (a) Reactor set up. (b) Temperature profile along the reactor. In (a), 1 - AsCl_3 bubbler; 2 - main ($\text{H}_2 + \text{AsCl}_3$) line; 3 - vapor etch line; 4 - vapor etch valve; 5 - Ga source; 6 - high temperature position of the substrate; 7 - low temperature position of the substrate (growth position); 8 - oil bubbler at exhaust; 9 - push rod to adjust the position of the substrate (hollow to allow insertion of a thermocouple to monitor the substrate temperature); 10 - reactor tube; and 11 - furnace. All the reactor parts going into the furnace are made of Spectrosil quartz.

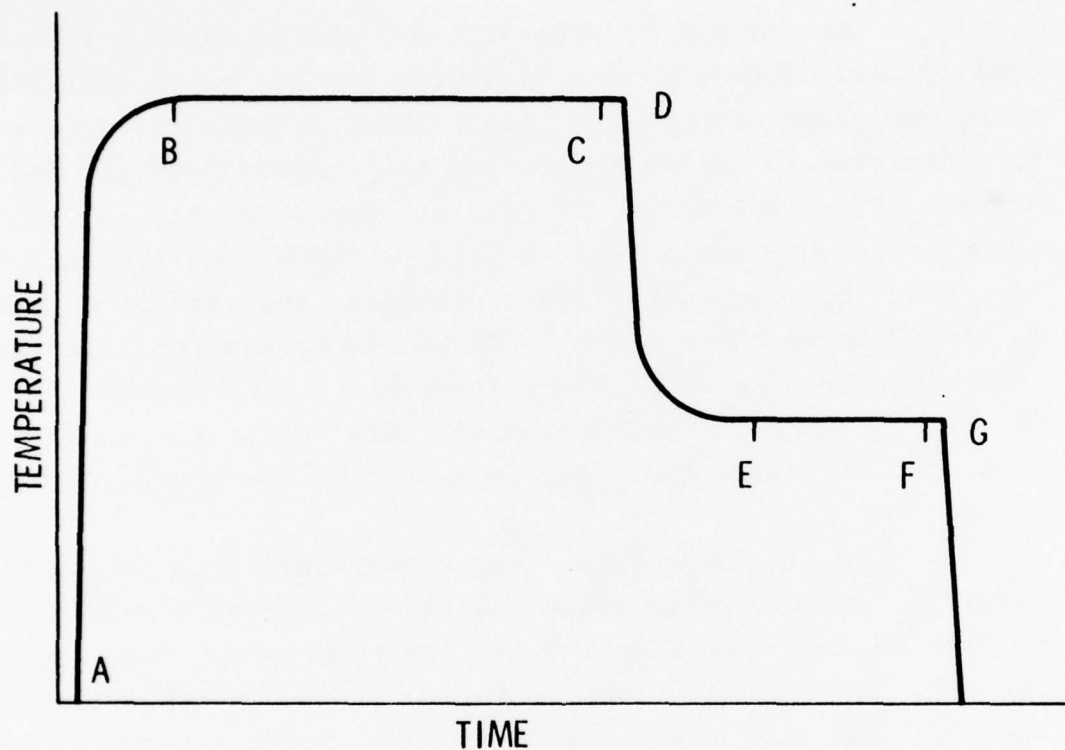


Fig. 2. Substrate temperature cycle during a typical growth run. AB - thermal equilibration; BC - source resaturation; CD - High temperature vapor etch of the substrate; D - point at which the substrate is pulled to the deposition position; DE - low temperature etch of the substrate; E - point at which the vapor etch valve is closed; EF - epitaxial growth; F - point at which the AsCl_3 flow is terminated; and G - point at which the furnace is rolled off.

During resaturation when the crust completely covers the Ga source, there is a pronounced change in the gas phase composition leading to etching conditions at the substrate. Figure 3 describes this situation quantitatively.

At the end of resaturation, the ($\text{H}_2 + \text{AsCl}_3$) flow is equally divided between the Ga source and the vapor etch lines using the vapor etch valve. After about 1/2 min of vapor etch, the substrate is pulled to the low temperature position and the total H_2 flow reduced to 330 cc/min. The substrate is vapor-etched at a very small rate in this position. After about 5 min to establish steady-state conditions, the vapor-etch valve is closed to initiate growth. Growth is terminated later by diverting the H_2 flow directly into the reactor instead of through the AsCl_3 bubbler. The furnace is rolled off after about a minute to allow the entire AsCl_3 gas to be purged out of the reactor.

By having a second low temperature bath for controlling the AsCl_3 bubbler temperature and allowing this to supply the coolant to the bubbler during the low temperature etch and growth, the AsCl_3 mole fraction can be varied during growth without changing the other conditions. With an AsCl_3 bubbler temperature of 20°C during growth, the background doping of the reactor used for this work is around $2 \times 10^{14}/\text{cc}$ (n-type) with a mobility of about $100,000 \text{ cm}^2/\text{V-sec}$ at 77K. The epilayer doping is obtained from Van der Pauw measurements and/or C-V measurements using a JAC impurity profile plotter.

Figure 4 gives the doping of the epilayer as a function of Sn content in the Ga source, the AsCl_3 bubbler temperature being 20°C . When the liquid phase epitaxial (LPE) process is used to grow the GaAs layer the corresponding data are also included for comparison. The latter also give the approximate Sn concentration in the GaAs crust formed over the Ga source

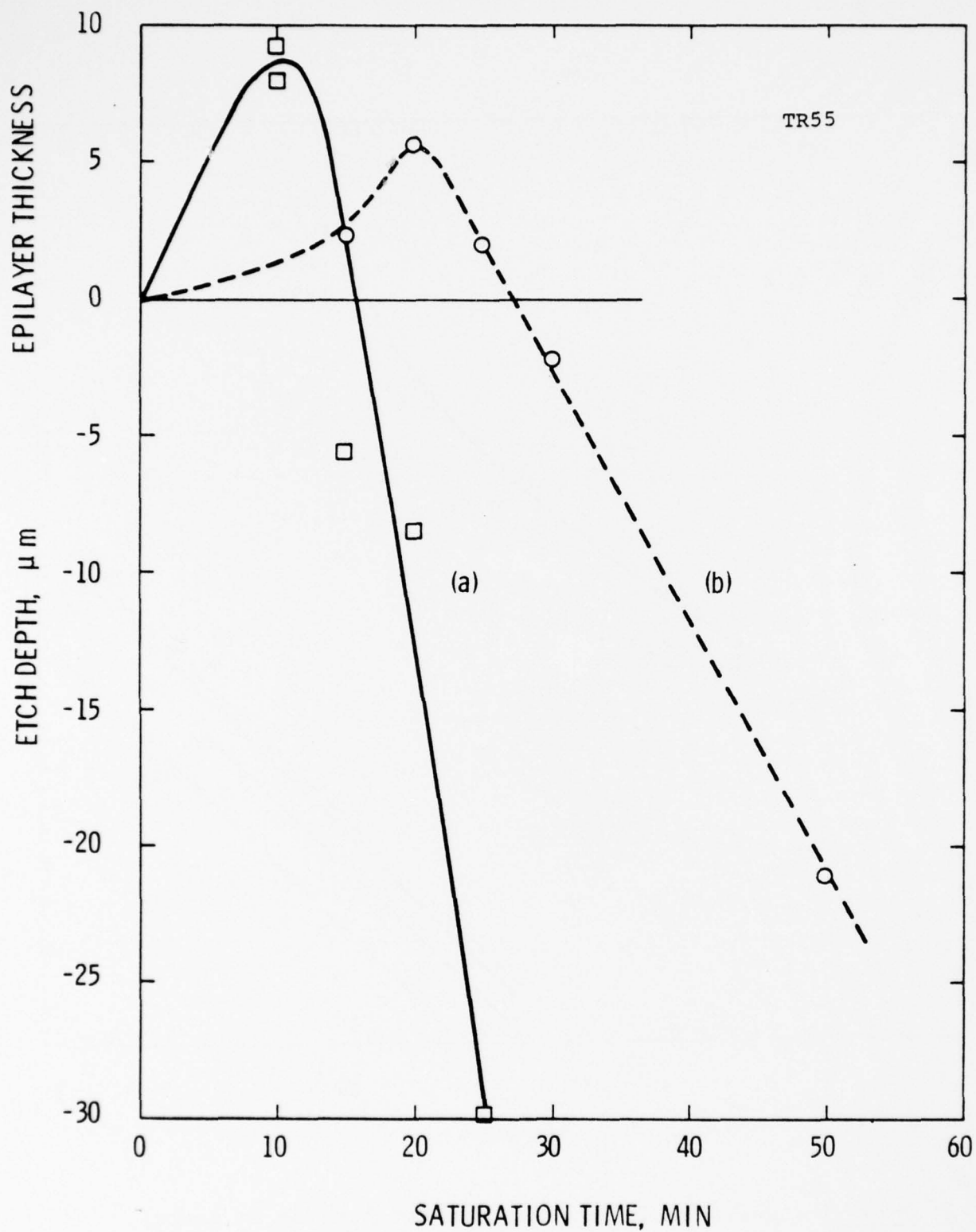


Fig. 3. Depth of etch vs saturation time, when AsCl_3 bubbler is at 20°C : (a) for a total flow rate of 500 cc/min, and (b) for 330 cc/min. In both cases, the substrate is at the high temperature position.

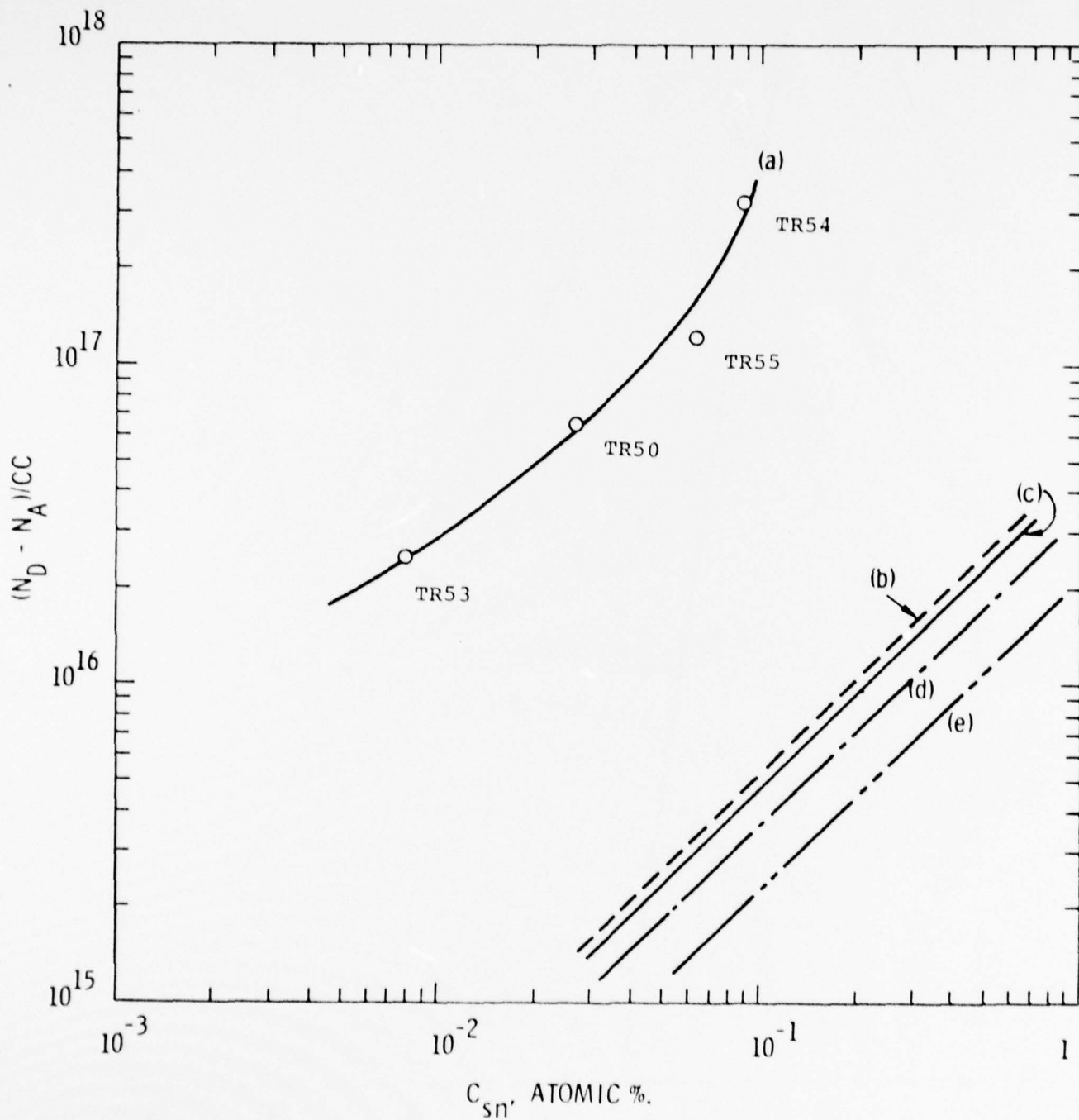


Fig. 4. Epilayer doping vs Sn content in the Ga source. (a) For VPE, (b) for LPE at 860°C , (c) for LPE at 780°C , and (d) for LPE at $725-730^{\circ}\text{C}$.

in the VPE system. Since the Sn content in the crust is very small compared to that in the (Ga+As) liquid solution underneath, a well saturated source with complete crust coverage is essential in obtaining reproducible epilayer doping.

The doping profile of two typical layers determined from the differential capacitance measurements are shown in Figs. 5 and 6 for N-ON and N-OFF HJFETs respectively.

2.1.2 Liquid Phase Epitaxial Growth

Germanium-doped p-type $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ and Ge-doped p^+ -type GaAs layers are grown by liquid phase epitaxy following the mesa formation on the active channel layer. Tin-doped active channel layers are about 0.35 micron and 0.14 micron for N-ON and N-OFF devices respectively as discussed in Sec. 1.1.1. Extreme care must be exercised to not back-dissolve such thin layers during the LPE growth. The boat and the growth parameters are optimized to overcome back-dissolving and to attain a high degree of reproducibility. To obtain and maintain a sharp $\text{Al}_{.5}\text{Ga}_{.5}\text{As}/\text{GaAs}$ p-n junction, Ge has been selected as the p-type dopant for its low diffusion coefficient ($\sim 10^{-14} \text{ cm}^2/\text{sec}$ at the growth temperature of 860°C). A cleaved and stained cross-section of LPE-grown layers having a thickness of 0.5 micron each is shown in Fig. 7.

The gate semiconductor resistance is determined by the conductivities and thicknesses of the p-type layers. For a small gate semiconductor resistance, the doping levels should be as high as attainable without reducing the layer quality. In addition, the thickness of the two p-type layers should be kept at a minimum. The p-AlGaAs layer thickness is nominally kept at 0.5 micron, below which bridging between the gate and the source and drain may take place. In the latter part of this

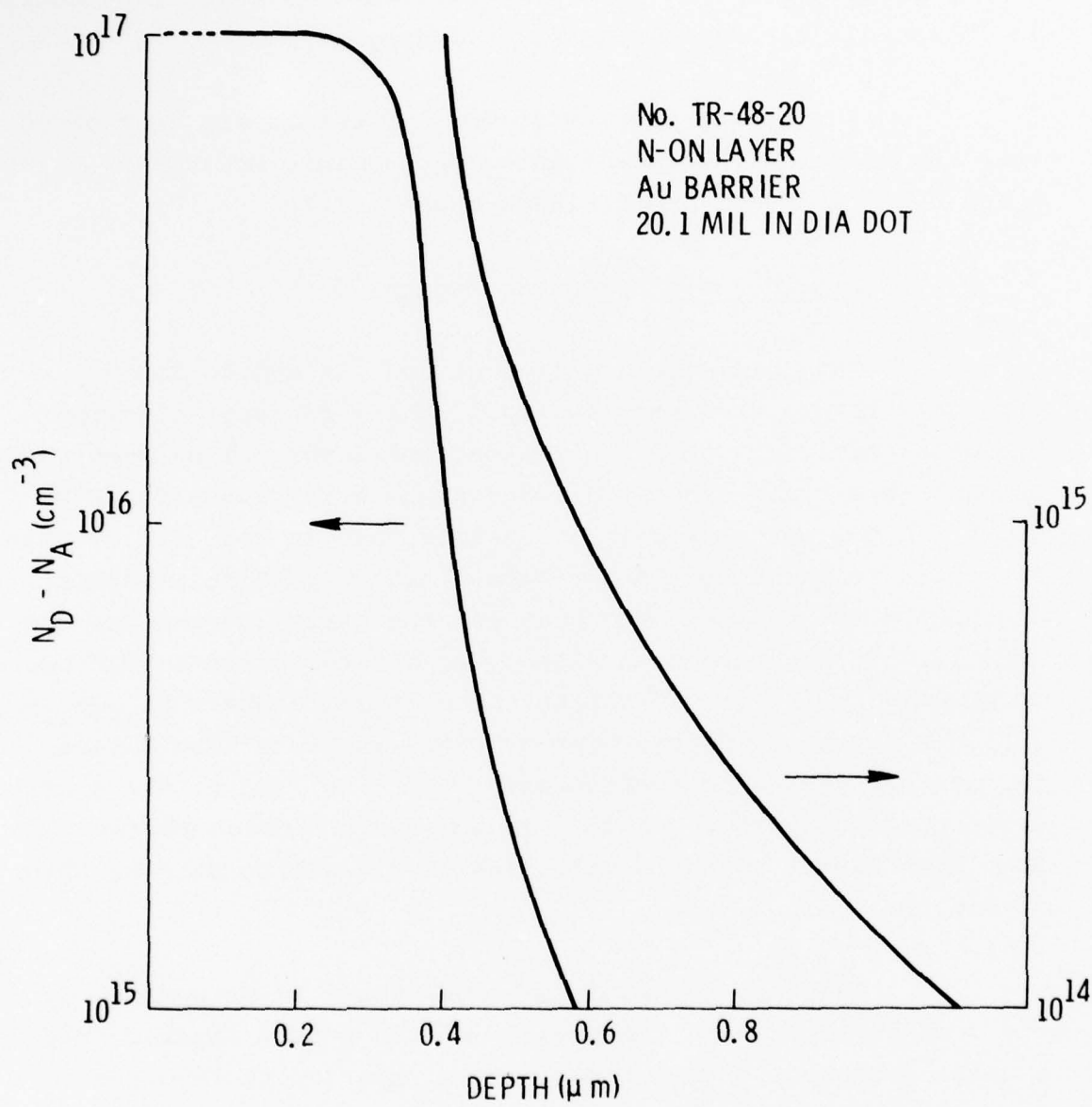


Fig. 5. Net donor concentration profile of an n-type GaAs epitaxial layer for N-ON HJFET applications.

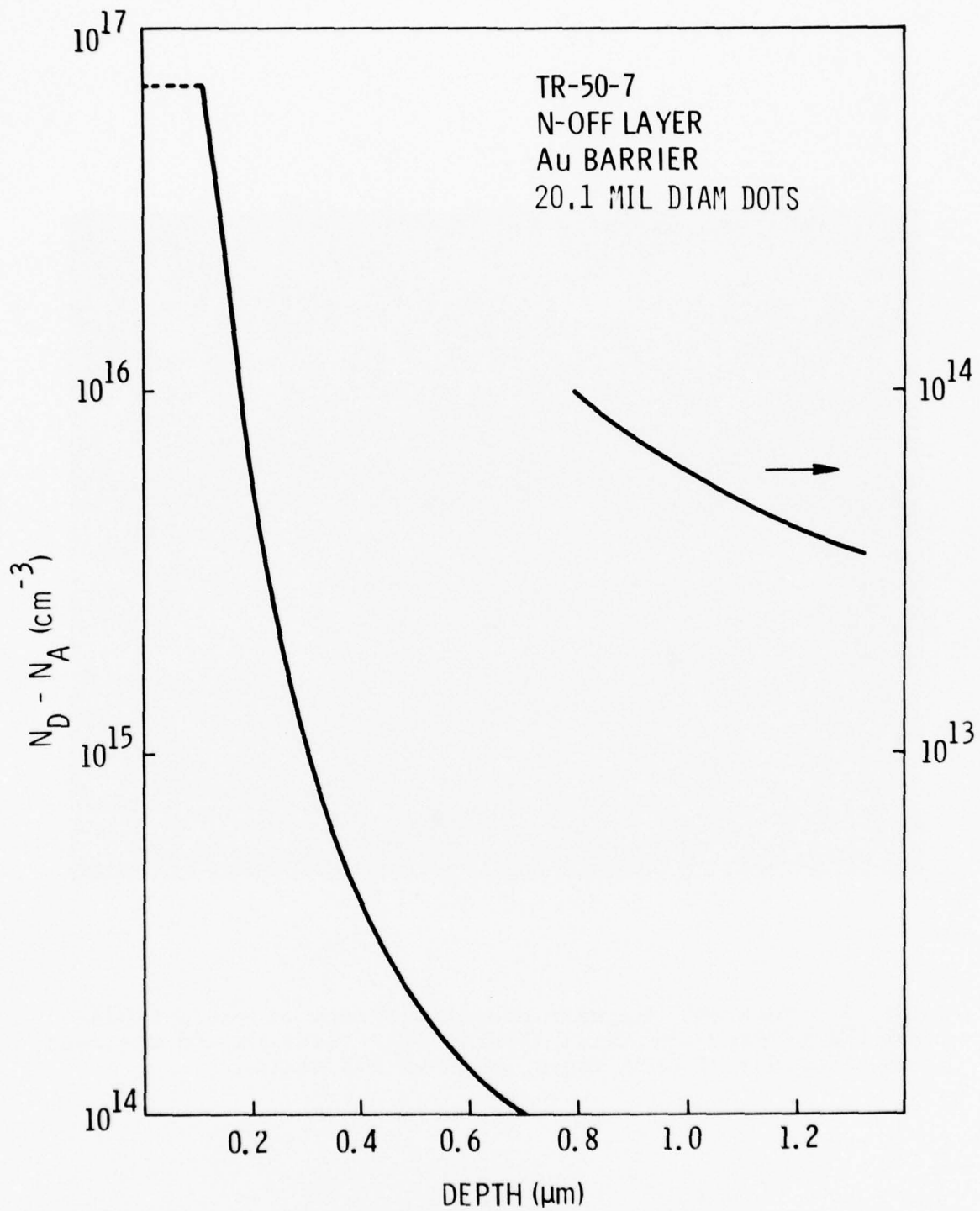


Fig. 6. Net donor concentration profile of a n-type GaAs epitaxial layer for N-OFF HJFET applications.

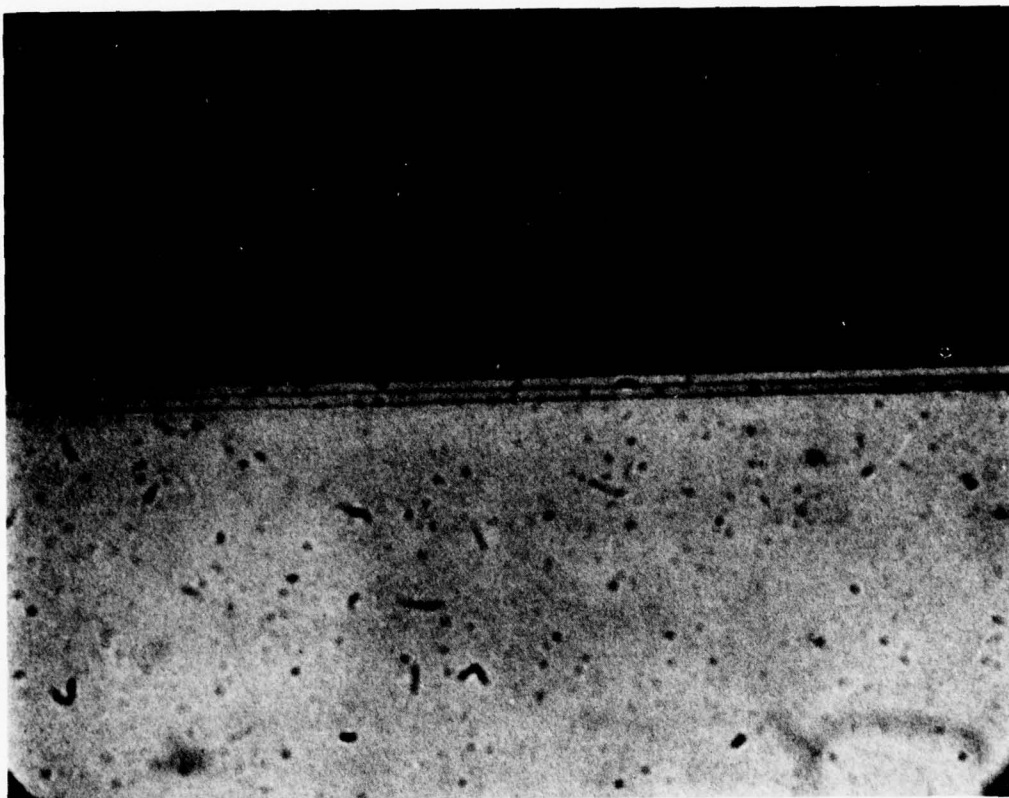


Fig. 7. Nomarski contrast photomicrograph of the p-AlGaAs and the p⁺-GaAs epitaxial layers after cleaving and staining. The thickness of each layer is about 0.5 micron.

work, the GaAs layer thickness typically was about 0.3 micron, which is sufficient in terms of both maintaining dimensional control by etching and its conductance. The solid solubility of Ge in GaAs with a planar interface grown at 860°C is $5 \times 10^{18} \text{ cm}^{-3}$, which is the limit for the net acceptor concentration if good surface quality is to be maintained. The low field mobility of such a layer is about $40 \text{ cm}^2/\text{V-sec}$. Addition of Al complicates the situation in that the incorporation of Ge in $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ is not independent of the Al content in the melt. Higher Al concentrations lead to lower Ge doping, making it difficult to achieve high net carrier concentrations. An acceptor concentration of about $2 \times 10^{18} \text{ cm}^{-3}$ has been achieved at the expense of back-dissolving the n-type active layer underneath. The devices fabricated using such a layer had ohmic source-gate and drain-gate junctions. SEM examination of a cleaved gate cross-section showed excellent gate formation, eliminating the possibility of external bridging as the cause. When the LPE-grown layers were selectively removed, the surface of the n-type layer looked rough as shown in Fig. 8 where the back-dissolving can easily be seen. This is attributed to a high Ge concentration in the melt, which is believed to form Ge inclusions at the bottom of the melt. These local Ga-rich Ge inclusions try to reach equilibrium by dissolving As from the n-type GaAs layer. Coupled with back-dissolving, Ge indiffusion also may have taken place. The Ge concentration of the AlGaAs layers has since been reduced to a level of 10^{18} cm^{-3} which led to the elimination of the surface degradation of the n-type GaAs as shown in Fig. 9. When the p-type LPE-grown layers are selectively removed from the field surrounding the mesas, the Cr-doped bulk material maintains its high resistivity, which is a good indication that any surface inversion layer is absent. The surface morphology of the Cr-doped field is the same as before it had undergone LPE growth cycle.



Fig. 8. Nomarski contrast photomicrograph of the n-type GaAs active layer after the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ having an acceptor concentration of $2 \times 10^{18} \text{cm}^{-3}$ has been removed by selectively etching. The magnification is 1400.



Fig. 9. Nomarski photomicrograph of the active layer after the removal of the $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ having a net acceptor concentration of $1 \times 10^{18} \text{cm}^{-3}$. Notice the back dissolving of the surface is eliminated. The apparent surface feature is that of the polished substrate which is replicated on the thin channel layer surface.

2.2 CONTACT POTENTIAL OF p-AlGaAs/n-GaAs HETEROSTRUCTURES

An accurate knowledge of the built-in potential is necessary before normally-off $\text{Ga}_{.5}\text{Al}_{.5}\text{As}$ gate heterojunction GaAs FETs can be designed. Therefore heterojunction $\text{Al}_{.5}\text{Ga}_{.5}\text{As}/\text{GaAs}$ p-n diodes, 345 microns in diameter, have been fabricated on an n^+ -type GaAs substrate. A vapor-phase-grown 0.2-micron-thick 10^{17}cm^{-3} epitaxial layer is first deposited on an n^+ GaAs substrate, followed by a LPE deposition of 10^{18}cm^{-3} Ge-doped 0.5-micron $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ and $5 \times 10^{18}\text{cm}^{-3}$ Ge-doped 0.5-micron GaAs. The heterostructure is formed by masking and selectively etching the p^+ -type GaAs and the underlying $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$. The contact metal evaporation on both sides of the wafer is alloyed at 450°C for 25 sec. The leakage current for the coplanar and noncoplanar diodes was measured and found to be in the low 10^{-9} A range. Capacitance measurements from -10 V to +1 V (note that the forward current for forward biases up to 1 V is negligible) have been made and a built-in voltage of 1.39 eV deduced from C^{-2} vs V data.² From measured forward I-V forward characteristics at room temperature,² the series resistance, the ideality coefficient, the saturation current, and the built-in potential have been calculated and found to be (in order) 1 ohm, 1.56, 1.6×10^{-15} A, and 1.36 eV (see Fig. 10(a)).

Since the homojunction theory does not apply in calculating the built-in potential, the discontinuities in the band diagram in addition to the density of states in the conduction and the valence band of $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ need to be known. Dingle et al.³ have reported that the conduction band discontinuity is 88% of the total bandgap difference between $\text{Al}_{1-x}\text{Ga}_x\text{As}$ and GaAs heterostructures. The other 12% of the total bandgap difference then gives the valence band discontinuity. The indirect bandgap of $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ is about 1.95 eV which implies a conduction band discontinuity (ΔE_c) of 0.466 eV by using Dingle's results.

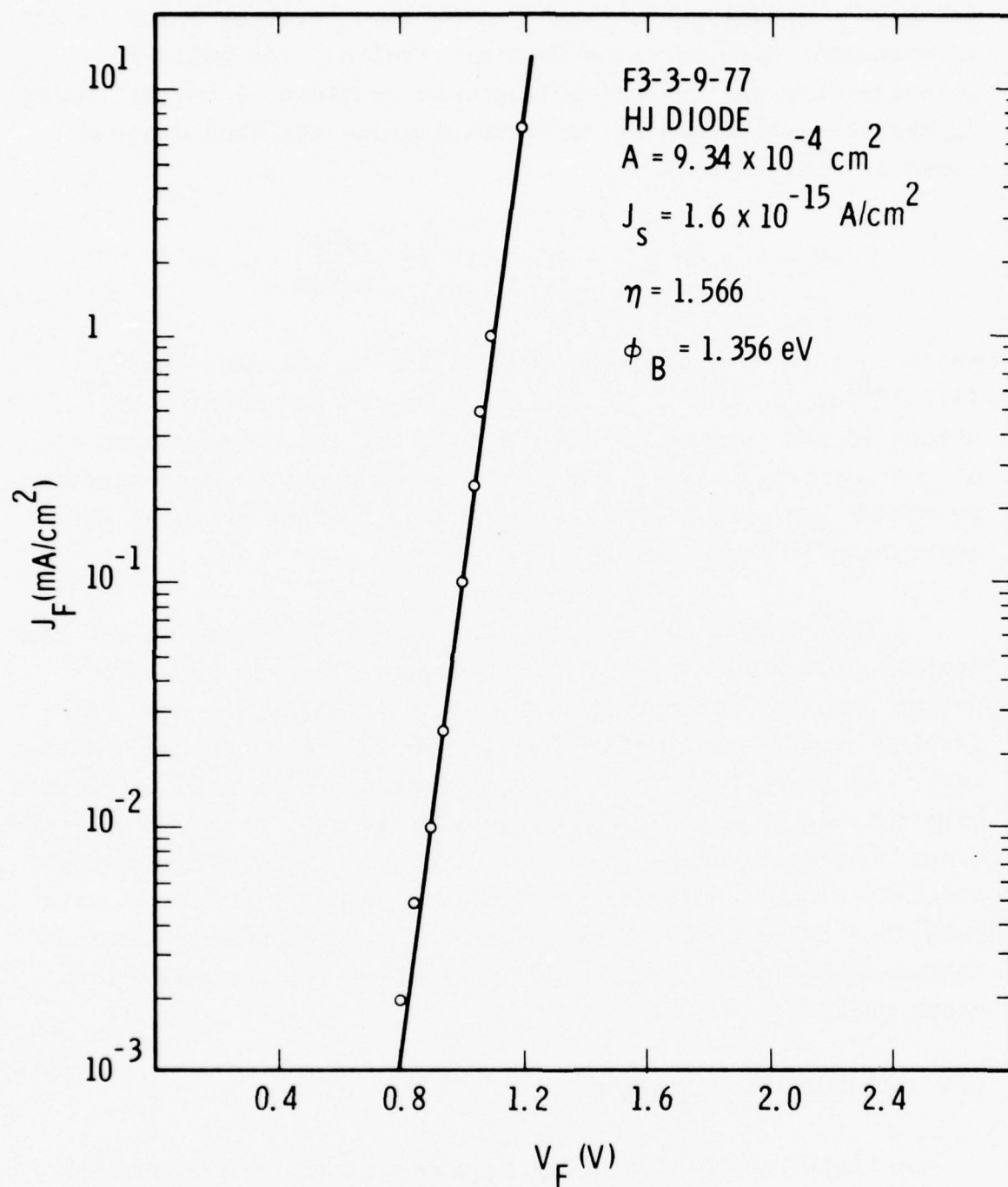


Fig. 10(a). Forward I-V characteristic of a heterojunction p-n diode used to calculate the diode parameters.

Anderson's⁴ model predicts ΔE_c to be about 0.28 eV which is not in agreement with our experimental results. The built-in potential for the heterojunction case is given by the following expression, which can be constructed using the band diagram shown in Fig. 10(b).

$$eV_{bi} = \phi_B = E_{g1} - \Delta E_c - kT \ln \frac{N_{c2} N_{v1}}{N_{A1} N_{D2}} \quad \text{in eV}$$

where E_g is the indirect bandgap of the $Al_{.5}Ga_{.5}As$, and N_{c2} ($4.7 \times 10^{17} \text{ cm}^{-3}$) and N_{v1} ($6.79 \times 10^{18} \text{ cm}^{-3}$) are the density of states in the conduction band of GaAs and the valence band of $Al_{.5}Ga_{.5}As$ respectively. N_{A1} is the net acceptor concentration in the $Al_{.5}Ga_{.5}As$ (10^{18} cm^{-3}) and N_{D2} is the net electron concentration in the GaAs (10^{17} cm^{-3}).

If the parameters using $Al_{.5}Ga_{.5}As$ and GaAs figures for the density of states are inserted in the equation, a built-in potential of approximately 1.393 eV is calculated. When the density of states of GaAs alone are used, the built-in potential comes out to be 1.394 eV. As can be seen, the density of states does not change the built-in potential as much as ΔE_c does. The close agreement between C-V, I-V, and calculated values using Dingle's results indicate that the ΔE_c used in the above calculations is correct. Finally, the results on heterojunction AlGaAs gate GaAs normally-off FETs confirm via the depletion depth that $\phi_B \approx 1.4$ eV.

2.3 FABRICATION TECHNIQUE

A liquid encapsulated (LEC) grown Cr-doped GaAs boule is sliced on the (100)-orientation with a thickness of 21 mils. The slices are then cookie-cut into 1-inch diameter substrates having a flat edge corresponding to one of the cleavage directions.

$$\begin{aligned}
 E_{g1} &= 1.95 \text{ eV} \\
 E_{g2} &= 1.43 \text{ eV} \\
 \Delta E_c &= 0.466 \text{ eV} \\
 \Delta E_v &= 0.064 \text{ eV} \\
 V_{D1} &= 0.22 \text{ eV} \\
 V_{D2} &= 1.33 \text{ eV} \\
 T &= 300^\circ \text{K}
 \end{aligned}$$

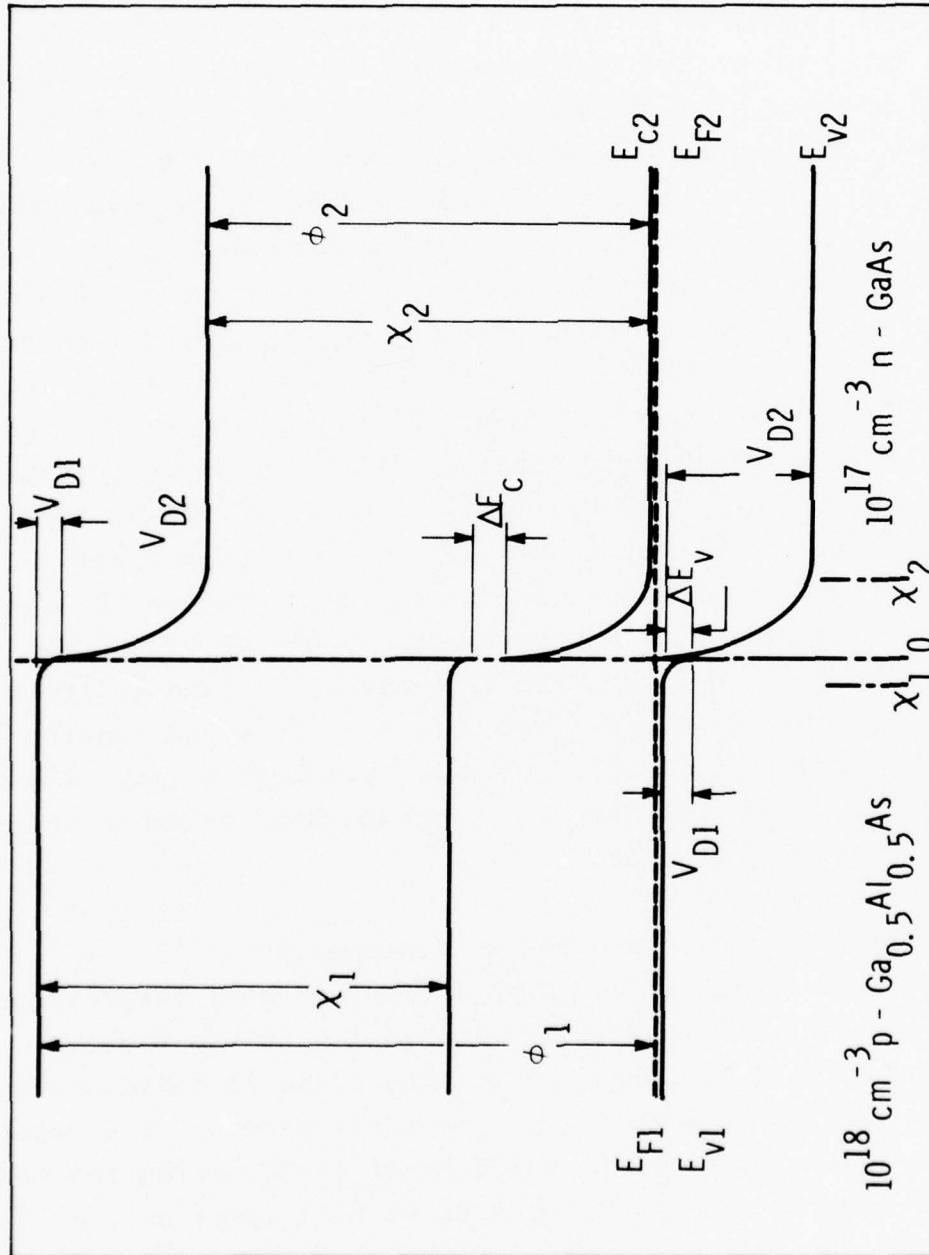


Fig. 10 (b). Band diagram of the $p\text{-Al}_{0.5}\text{Ga}_{0.5}\text{As}/n\text{-GaAs}$ heterojunction.

In this particular example, the flat edge runs along the $[0\bar{1}1]$ direction. The back side of the slices is diamond-lapped to flatten the surface, during which process about 1 to 2 mils of material are removed. The front side is also diamond-lapped and polished with a $\text{Br-CH}_3\text{OH}$ mechanical-chemical polishing technique until a final thickness of 15 mils is obtained. The substrate thickness is of great importance because of restrictions imposed by the LPE process. Too thin a substrate leads to poor melt removal that results in post-growth nucleation on the wafer locally or as a whole. After a thorough chemical cleaning and a slight in-situ high temperature etch as discussed in Sec. 1.1.1, 0.35-micron thick epilayers for N-ON and 0.14-micron thick epilayers for N-OFF HJFETs are deposited at 767°C . The net donor carrier concentration associated with both types of layers is about 10^{17}cm^{-3} . The layer thickness and the doping profile are deduced from room temperature differential capacitance measurements using Au dot Schottky barriers. Removal of the Au dots at the end of the C-V measurements is followed by mesa mask definition at which point a decision regarding the type of gate cross-section is desired. The mesa mask should be registered in a way that the resulting gates are parallel to the $[011]$ direction. On the other hand, inverted V-type gates would require an alignment along the $[0\bar{1}1]$ direction. Needless to say, the $[011]$ and $[0\bar{1}1]$ directions have to be established prior to mesa-mask generation on the wafer.

The field surrounding the mesas is etched in 3:1:1 ($\text{H}_2\text{O}:\text{HF}:\text{H}_2\text{O}_2$) or in 3:1:15 ($\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$) at room temperature until the semi-insulating material is reached in the field. After the removal of the photoresist, the wafer is immediately loaded into the LPE reactor for p-type layer growth. The wafer undergoes a hot cycle of about 1-1/2 hr at 860°C during the LPE growth of p-type $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ doped with Ge to a level of 10^{18}cm^{-3} and of p⁺-type GaAs doped with Ge to a net donor con-

centration of $5 \times 10^{18} \text{ cm}^{-3}$. A slight supercooling is applied prior to the contact between the Al-Ga-As melt and the wafer to avoid back-dissolving the active layer. The LPE-grown layers are about 0.5 micron each, however a thinner p^+ GaAs layer would be desirable, for increased dimensional control during the formation of the gate.

The p^+ -GaAs and p-AlGaAs layers are selectively removed in two narrow stripes on two ends of the wafer to delineate the mesas to be used for the alignment purposes during gate mask exposure. The 5x300 micron gate pattern is then defined using Shipley AZ1350J photoresist. The p^+ "cap" layer is etched selectively in pH 7.05 superoxol ($\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$) with a slight agitation. This process is continued until a cap layer dimension of about 1.5 to 2.0 microns is achieved, which determines the channel length of the final device. It should be pointed out that the etching rate is a function of the degree of agitation and the age of the mixed chemicals. Typically, a freshly mixed pH 7.05 solution removes 0.5 micron of material in about 7-10 min under the agitation conditions used. To complete the gate structure, the AlGaAs layer is selectively etched in room temperature HF. The etching process is continued until the AlGaAs is completely removed from the field and the necessary undercutting to provide self-alignment is achieved. AuGe/Ni/Au metallization is then deposited and alloyed at 450°C for 25 sec to form the n-type and p-type contacts for the source-drain and the gate respectively.

To further reduce the gate resistance, several attempts were made to use Au/Mg/Au to provide a better contact material for the p-type GaAs, while maintaining AuGe/Ni/Au for the n-type GaAs. The p-type gate metallization is done first. Two-micron wide Au/Mg/Au stripes are evaporated and lifted off, followed by a 7x300 micron photoresist gate pattern aligned over the Au/Mg/Au gate fingers. The rest of the steps are exactly the

same as described above. About 2000 \AA of Au metal is evaporated on the source, drain and gate bonding pads by the lift-off technique to facilitate bonding. The back side of the substrate is then polished to achieve a final wafer thickness of 150 microns and about 2000 \AA of electroless Pd is plated on the back side. The devices are scribed and diced-up. For dc and high speed measurements, the devices to be tested are die-bonded on a gold-plated copper block with a AuSn preform. Each source pad is bonded to ground with double 0.7-mil Au wire while the gate and the drain are bonded with 0.7-mil Au wires to the input and the output lines respectively. The 50-ohm input and output lines are formed on an easily machineable Duroid substrate. The fabrication steps are summarized in Fig. 11.

2.4 EXPERIMENTAL RESULTS AND TEST PROCEDURES

2.4.1 Gate Formation

As discussed in the previous section the $\text{NH}_4\text{OH}/\text{H}_2\text{O}_2$ etch with a pH value of 7.05 (superoxol) is used to etch the p^+ GaAs contact layer. The superoxol has been found to have the lowest undercutting rate among $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ (5:95), $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (5:5:90) and 1 molar $\text{NaOH}:\text{H}_2\text{O}$ (20:1). In addition, the superoxol and $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2$ (5:95) are the only ones that do not attack $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$, while the others exhibit a much smaller etching rate in $\text{Al}_{.5}\text{Ga}_{.5}\text{As}$ compared to GaAs. It should be pointed out that the etches listed above are only a small fraction of the solutions that have differential etching rates for GaAs and AlGaAs. Since the superoxol proved to be satisfactory for the application we are concerned with, further experimentation with other etches was discontinued.

In addition to having a selective etching property, the etch used to form the gates should maintain straight line

HJFET FABRICATION STEPS

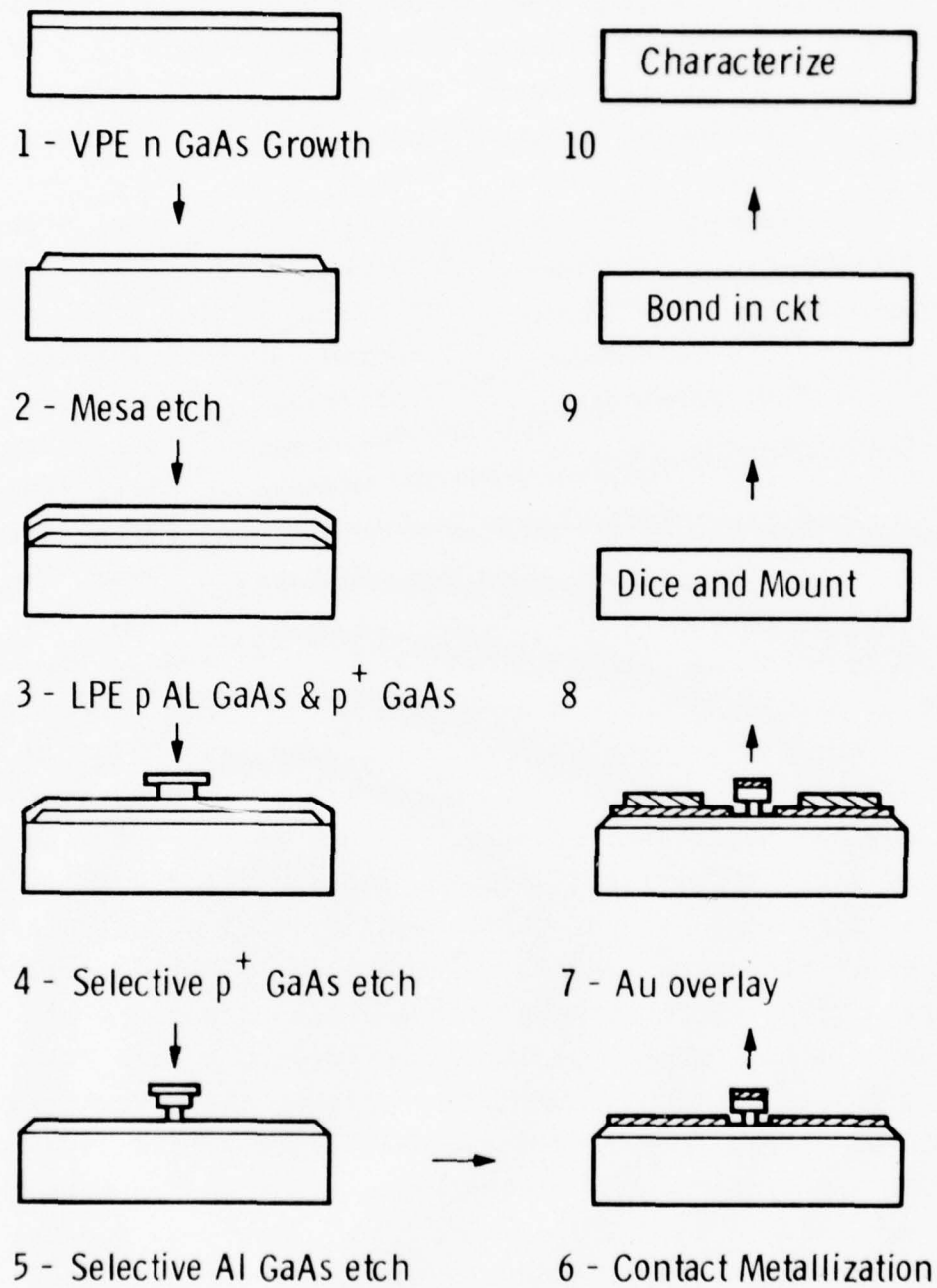


Fig. 11. Fabrication steps of the heterojunction FET.

definition without any signs of bowing. Figure 12 illustrates a gate finger pattern near the gate pad that has been formed by etching the GaAs from the field 4 microns deep. The finger which is still covered by the photoresist is about 1.5 microns wide as opposed to the original photoresist dimension of 3.5 microns. This implies an undercut-to-etch ratio of about 0.25.

In order to control the gate cross-section the $[011]$ direction needs to be distinguished from the $[0\bar{1}1]$ direction. Aligning the gates parallel to $[011]$ and the $[0\bar{1}1]$ directions result in V-type trapezoid and inverted V-type trapezoid gate cross-sections respectively. Consequently, the gate should be parallel to the $[011]$ direction to achieve ultra-small gate lengths. $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (3:1:15) is used to identify the $[011]$ direction from the $[0\bar{1}1]$ direction on one edge of the wafer. In some instances, 1% $\text{Br}-\text{CH}_3\text{OH}$ has been used instead, but found to be not as reproducible. Figure 13 shows the top view of one of the etch pattern obtained with 3:1:15 and its cross-section taken perpendicular to the long edge of the etch pattern. To achieve the V-type gate cross-section requires the mesas be aligned in such a way that the gates are perpendicular to the long edge of the etched pattern. Figure 14 shows a gate profile aligned along the $[0\bar{1}1]$ direction, showing clearly the inverted V-type trapezoid. On the other hand, Fig. 15 illustrates the case where the gates are aligned along the $[011]$ direction. Unfortunately, the thickness of the AlGaAs layer and the channel length were not properly selected to produce a well defined V-shaped cross-section in this case. Either the channel length should have been longer or the AlGaAs layer should have been thinner. Therefore, the AlGaAs layer thickness in subsequent runs was reduced to 0.5 micron or less. However, the thickness of the contact metallization imposes a lower limit of about 0.3 micron to eliminate shorting of the source to the p^+ GaAs gate cap by the metallization.

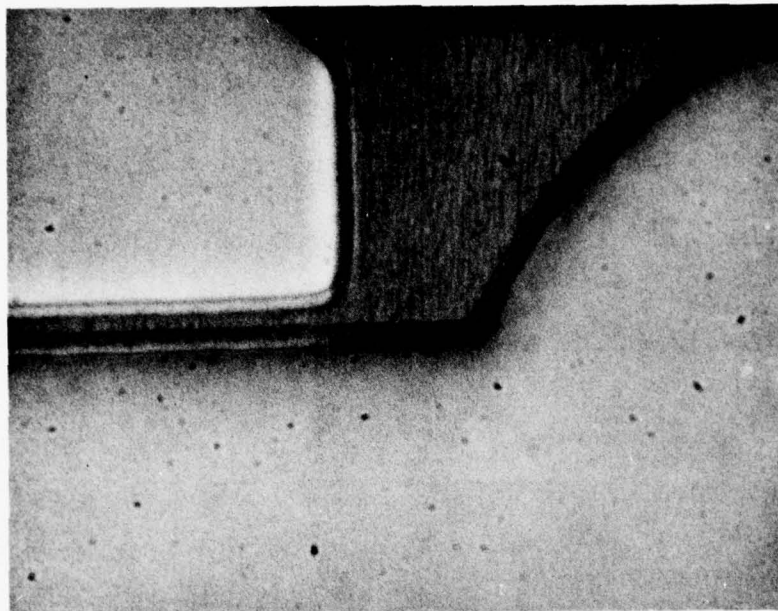


Fig. 12. Line definition obtained by pH 7.05 $\text{H}_2\text{O}_2:\text{NH}_4\text{OH}$ (superoxol). The original line defined by the photoresist is about 3.5 microns wide. After etching 4 microns down, a final width of 1.5 microns is achieved indicating about 25% undercutting on one side.

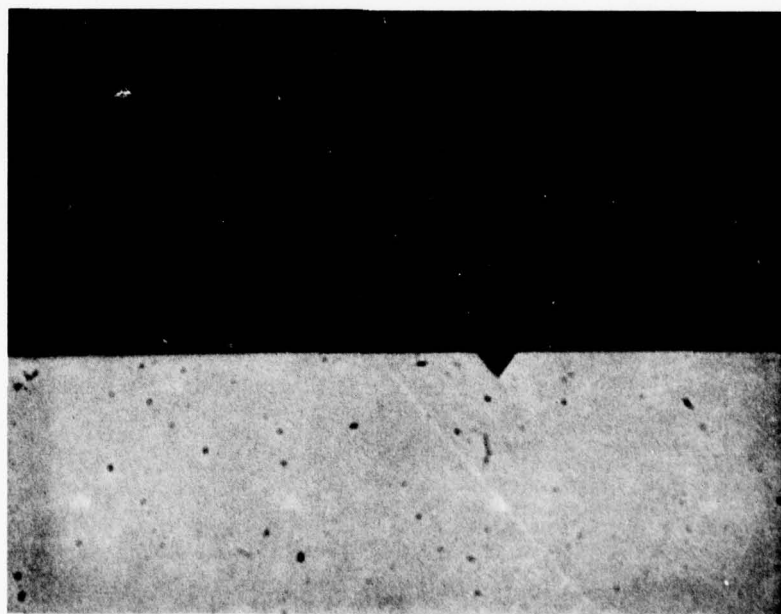
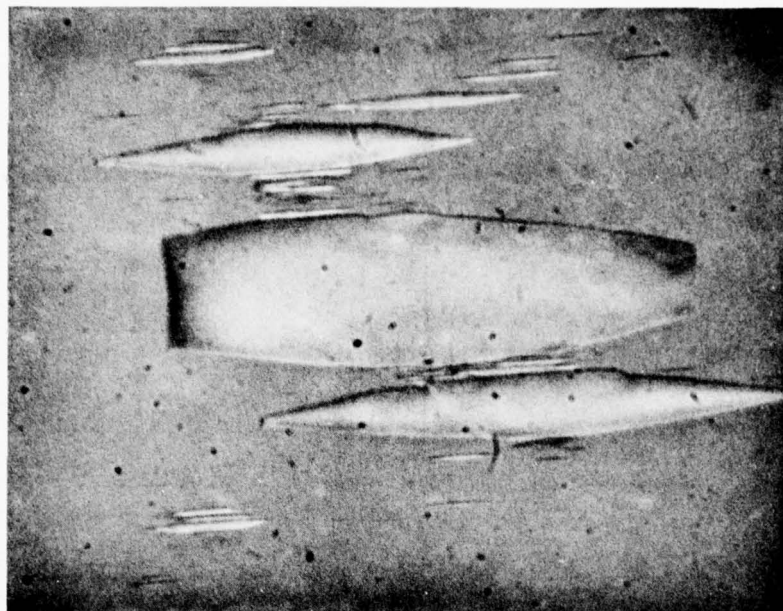


Fig. 13. Etch pattern (top) of $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (3:1:15) on (100) GaAs and its cross-section (bottom) taken perpendicular to the longer edge. Longer edges of the patterns are parallel to the [011] direction.



Fig. 14. SEM photograph of a gate cross-section showing inverted V-type profile. Clearly, the gate is aligned along the $[011]$ direction. AuGe/Ni/Au metallization also can be seen. The magnification is about 11,500x.

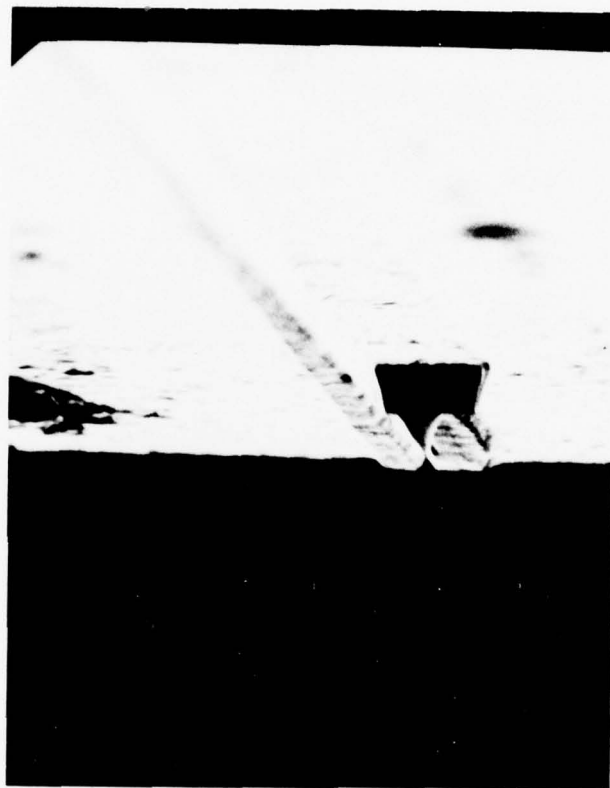


Fig. 15. SEM photomicrograph of a gate aligned along the $[011]$ direction. The channel length and/or the thickness of the AlGaAs layer is not properly chosen to obtain a well defined V-type cross section. Magnification is about 6250.

2.4.2 Contact Resistivity Studies

The specific contact resistance (r_c) of AuGe/Ni/Au metallization on n-type (10^{17} cm^{-3}) and p^+ -type ($5 \times 10^{18} \text{ cm}^{-3}$) GaAs are measured utilizing contact pads that are 250 microns long and spaced at a distance varying between 1 and 20 microns from one another. Low 10^{-6} ohm/cm^2 values for n-type and $1-2 \times 10^{-4} \text{ ohm/cm}^2$ for p-type are obtained after alloying at 450°C for 25 sec. Although lower values of the r_c on p-type GaAs with AuGe/Ni are obtained by reducing the alloying time, the first priority was given to reducing the source resistance.

AuMg can be used to reduce r_c on the p-type GaAs while AuGe/Ni/Au is used on the n-type GaAs. In this case, however, processing steps are different in that the AuMg gate pattern is deposited first and the p^+ -GaAs and p-AlGaAs are etched, later followed by an overall AuGe/Ni/Au evaporation. Using 4% AuMg (alloyed in-house using 0.999 Mg) and a 450°C , 25-sec alloy, a specific contact resistivity of $5 \times 10^{-6} \text{ ohm-cm}^2$ is obtained on $5 \times 10^{18} \text{ cm}^{-3}$ p-type GaAs and approximately $1-2 \times 10^{-5} \text{ ohm-cm}^2$ on 10^{17} n-type GaAs. When the Mg content is reduced to 0.3%, the Schottky-barrier characteristic obtained on n-type GaAs indicates that the impurities in the Mg are responsible for the ohmic contact on n-type GaAs since Mg is a well-behaved acceptor. This experiment, however, was not repeated on p-type GaAs.

From the discussion above, one concludes that to lower the gate resistance without sacrificing the source resistance, separate metallizations for the gate and the source should be performed, unless the doping of p^+ -GaAs and/or the structure of the contact metallization are changed.

Using only the AuMg metal as a mask to etch the GaAs and AlGaAs introduces new constraints on the thickness of the

epilayers. In this case the line width should be about 1.5 to 2 microns, and very thin layers are required. Moreover, the integrity of AuMg cannot be maintained while etching in a pH 7.05 since the Mg is attacked, resulting in metal liftoff. Thus to protect the metal, a 7-micron wide overlapping AZ1350J photore-sist pattern is put down over the 2-micron wide AuMg metal. However, as illustrated in Fig. 16, when the gate pattern is etched, the undercutting becomes large and irregular. This may be due to an electro-chemical potential which causes a depletion layer which in turn is attacked by the solution at a remarkably faster rate. The GaAs material used for this experiment is Cr-doped, and using p^+ GaAs material may reduce the undercutting to some degree. Further experiments need to be carried out to establish the mechanism of undercutting.

The channel length of the finished devices can be measured under an optical microscope. However, the same procedure cannot be applied to the gates. Therefore, the p^+ GaAs cap is broken to allow one to measure the approximate gate length with an optical microscope. Due to submicron gate lengths involved, a clean cleavage of the gate cross-section could not be achieved. Illustrated in Fig. 17 is the top view of a finished device at a magnification of 296.

Fig. 18(a) shows an uncovered AlGaAs gate which measures less than 0.5 to 0.7 micron and Fig. 18(b) shows a close-up view of the gate near the gate pad. The gate periphery is 300 microns and the channel length is about 2.5 to 3 microns with an associated gate length of about 0.5 to 0.7 micron.

2.4.3 Normally-On FJFET Device Results

DC measurements have been utilized to deduce the drain saturation current (I_{DS}), the source resistance (R_S), the drain



Fig. 16. SEM photomicrograph of a gate cross section during the early stages of the GaAs etching process in the presence of a 2-micron wide AuMg stripe (bright area embedded in the photoresist). The top 7-micron wide stripe is a AZ1350J photoresist pattern. Undercutting towards the metal is intolerably high.

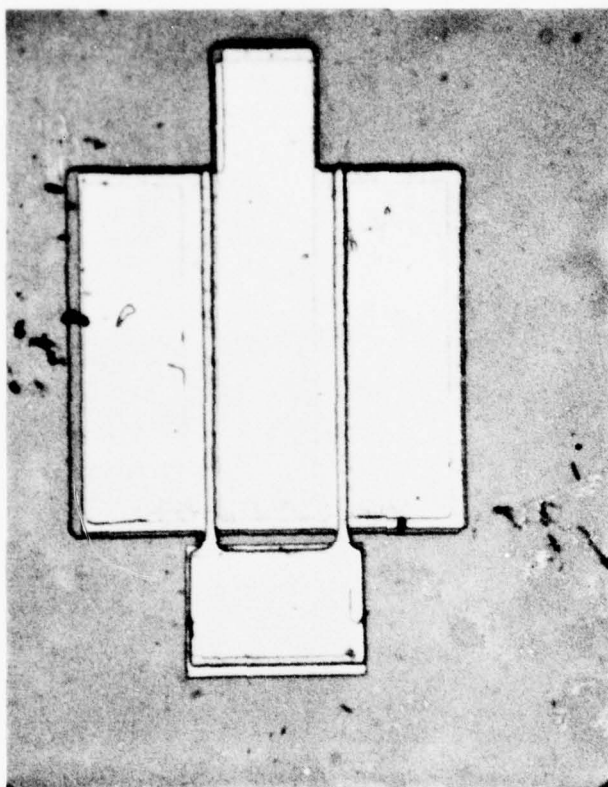


Fig. 17. Top view of a completed HJFET.

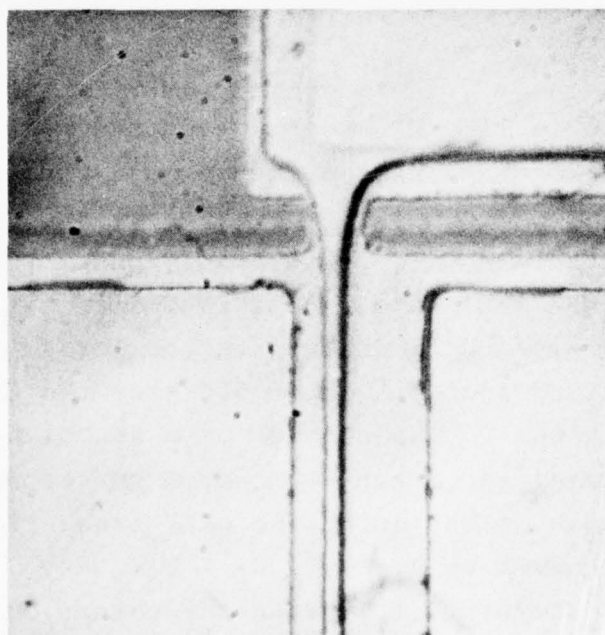
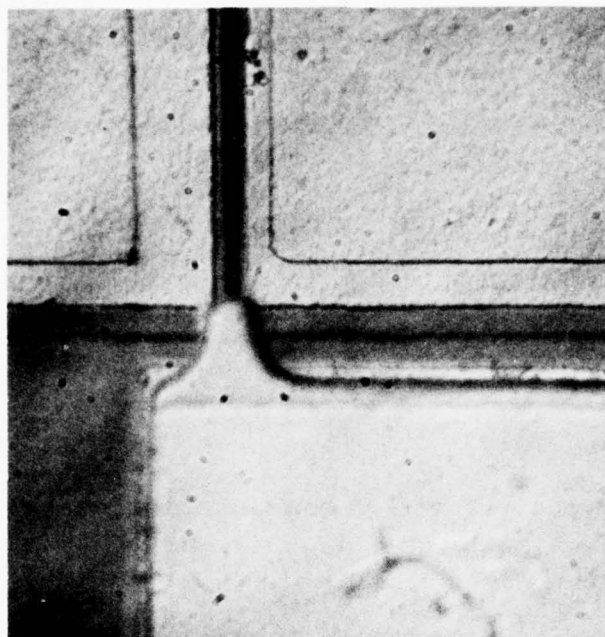


Fig. 18. (a) Photomicrograph of a HJFET with an intentionally broken cap layer. The dark line is the AlGaAs gate which is estimated to be about 0.5-0.7 micron. (b) Photomicrograph of the complete gate structure near the gate pad.

resistance (R_D), the gate resistance (R_G), the source-drain resistance (R_{S-D}), and the dc transconductance (g_m). The values obtained are as follows:

$$\begin{aligned} R_G &= 15 \text{ ohms} \\ R_S &= R_D = 5 \text{ ohms} \\ R_{S-D} &= 10 \text{ ohms} \\ I_{DS} &= 100 \text{ mA} \\ g_m &= 20\text{-}25 \text{ mmhos} \end{aligned}$$

Figure 19 shows the drain I-V characteristics of such a device with an associated gate periphery of 150 microns (1/2 the device). Shown in Fig. 20 is the gate-source I-V characteristic where the leakage current at -10 V is 10 μ A. By drying the devices in a H_2 ambient at about 300°C for a short time, this leakage current can be reduced.

Shown in Fig. 21 are the saturation drain current and the associated dc transconductance as a function of the gate bias for a N-ON HJFET. Since velocity saturation is achieved, the transconductance should be inversely proportional to the square root of the gate bias. This is indeed satisfied between 0 and -4 V. However, g_m decreases faster for $V_g < -4$ V, indicating severe velocity degradation within 500 Å of the interface. Velocity of the electrons in the channel as a function of depth is calculated using the drain saturation current as a function of the square root of the effective gate bias. The effective gate voltage is given by $V_{bi} + I_{DS}R_S + E_M L_g - V_g$, where V_{bi} is the contact potential, I_{DS} drain saturation current, R_S source resistance, E_M critical electric field (3.5 kV/cm for GaAs) above which the velocity saturates, L_g gate length, and the applied gate voltage (negative for N-ON HJFETs). Figure 22

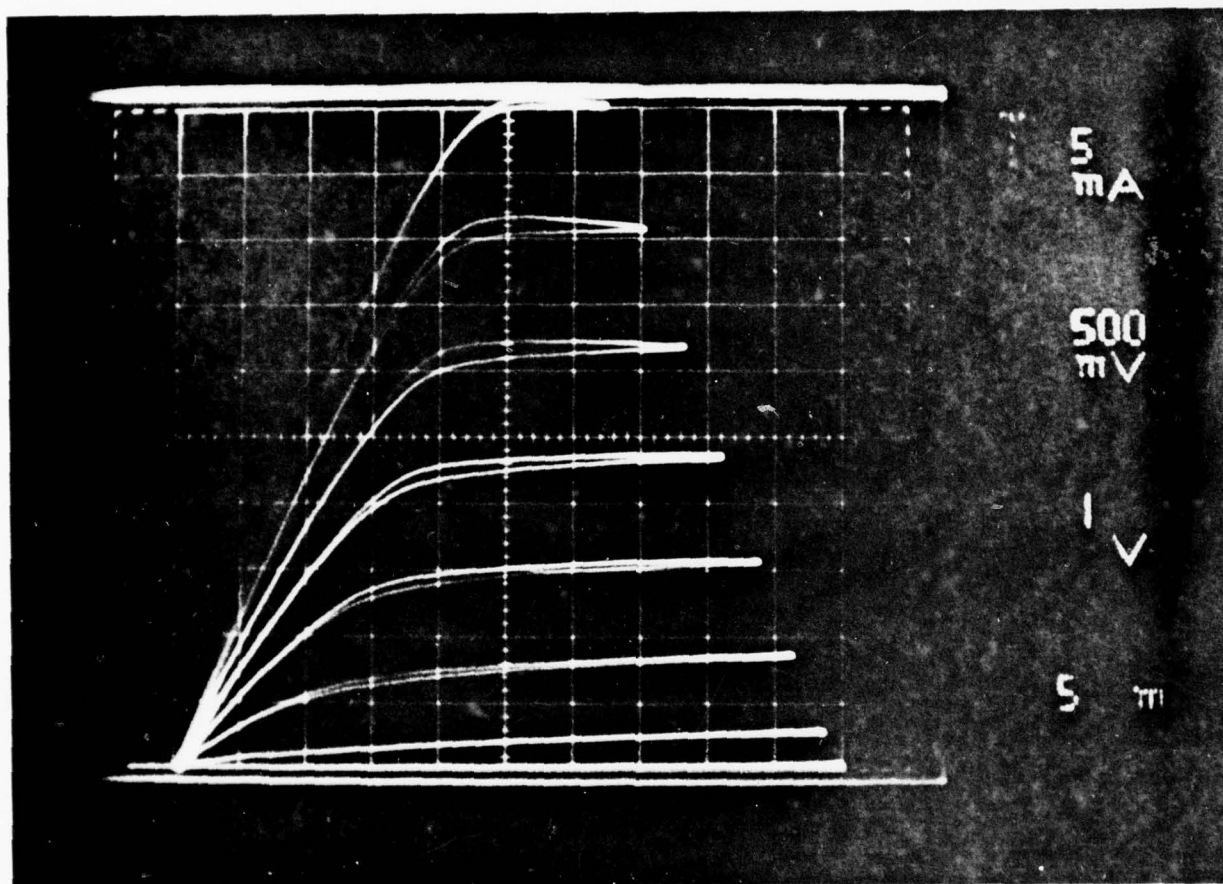


Fig. 19. Drain I-V characteristics of a N-ON HJFET with associated gate periphery of 150 microns (1/2 device).

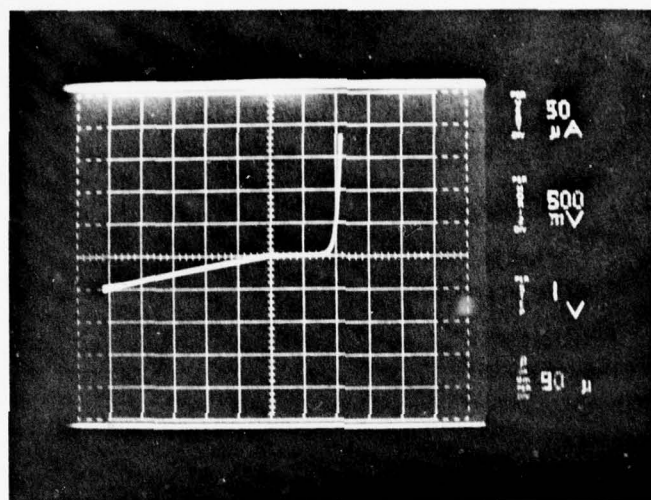


Fig. 20. Gate-source diode I-V characteristic of a N-ON HJFET. (500 mV/div and 50 μA /div in the forward, and 2 V/div and 10 μA /div in the reverse directions).

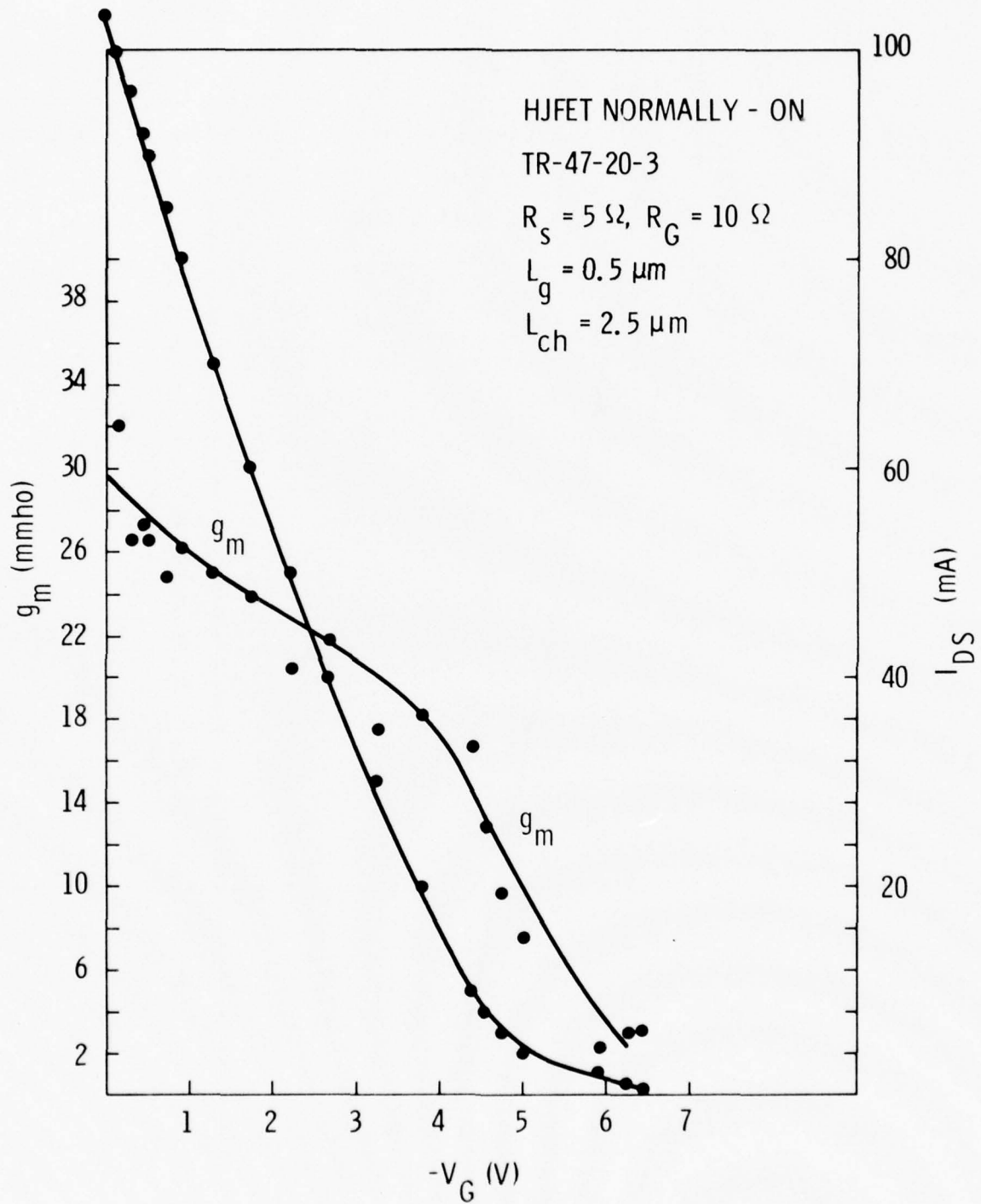


Fig. 21. Saturation drain current and the associated dc transconductance of a N-ON HJFET as a function of the reverse gate bias.

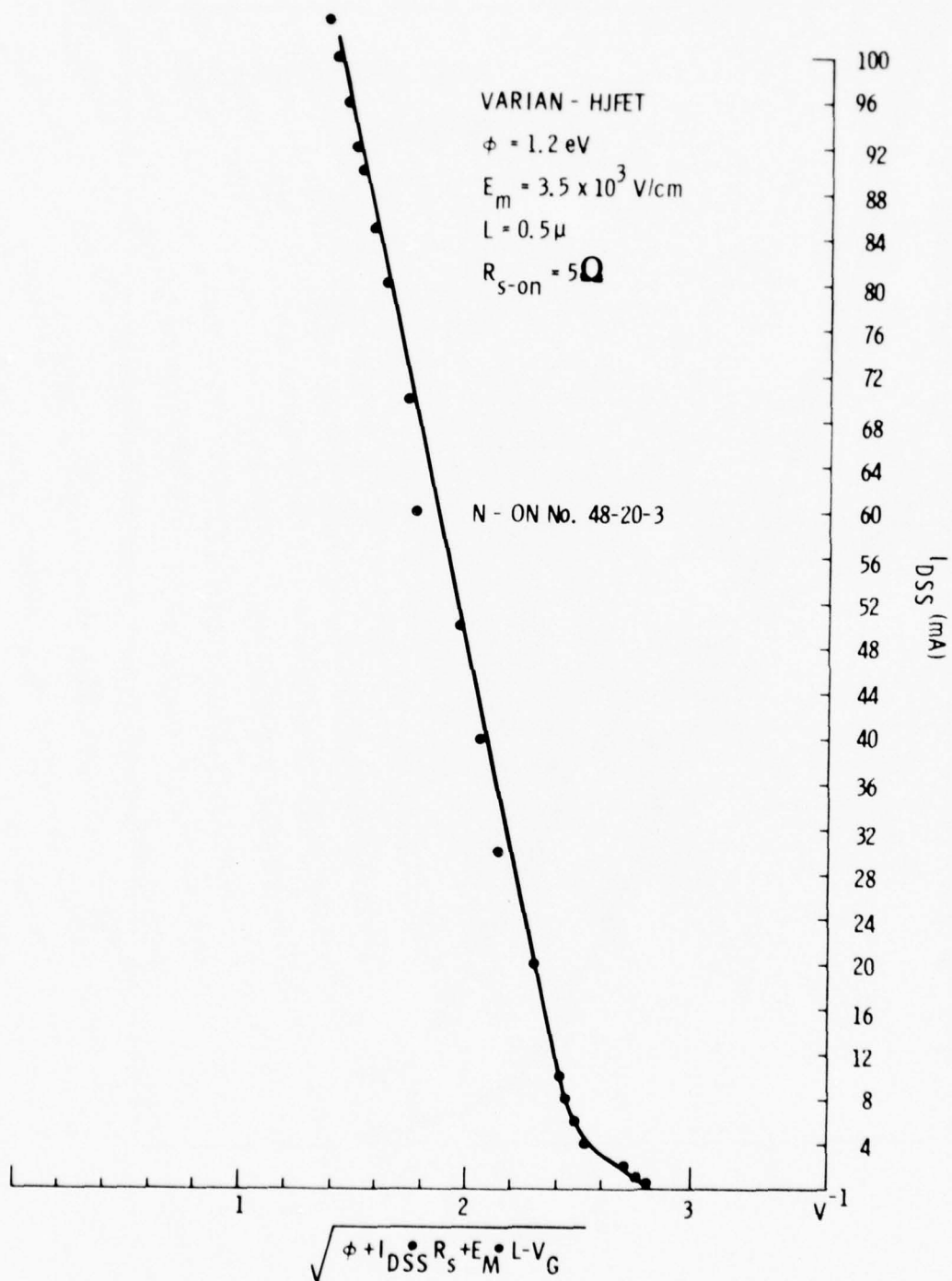


Fig. 22. The saturation drain current of a N-ON HJFET vs the square root of the effective gate bias. The slope of this curve can be used to calculate the velocity of the electrons.

is a plot of the saturation drain current as a function of the square root of the effective gate voltage ($\sqrt{V_{\text{eff}}}$), the slope of which can be used to calculate the saturation velocity as a function of depth into the channel layer as described in the Appendix. Figure 23 shows the saturation velocity profile of the electrons in the channel deduced from Figure 22.

Small signal S-parameter measurements covering a range of 2-14 GHz were made using a precalibrated 50-ohm microstrip fixture. The results are given in Tables I, II and III. N-ON devices with a gate length of approximately 0.5 micron exhibited a calculated maximum available gain (MAG) of 9.5 dB at 8 GHz from the S-parameters and a measured MAG of about 8.5 dB at 8 GHz (Fig. 24). S_{11} and S_{22} parameters associated with the above N-ON HJFET are shown on the Smith Chart in Fig. 25. The looping in S_{11} is attributed to the calibration errors and resonance effects in the input circuit. In this particular case, the input lead inductance appears to be relatively high, making S_{11} inductive at the higher frequency edge of the range of interest. Figure 26 shows the equivalent circuit model calculated from the measured S-parameters. The lead inductances are calculated from the physical dimensions and taken into account in computing the input and the output parameters. The feedback resistance component could be deduced from the computer optimization, which we have not pursued however. The input resistance is high compared to a similar N-ON Schottky barrier FET. This gate resistance compares well with the calculated 13-ohm gate resistance calculated using the measured specific contact resistivity of the cap layer and the resistance components contributed by the gate and the cap semiconductors. A different dopant such as Mg could be used to increase the doping concentration of the GaAs cap layer well into 10^{19} cm^{-3} range to reduce the specific contact resistance.

The stability factor K is given in Table III for N-ON and Table VI for N-OFF HJFET at each measured point. Although

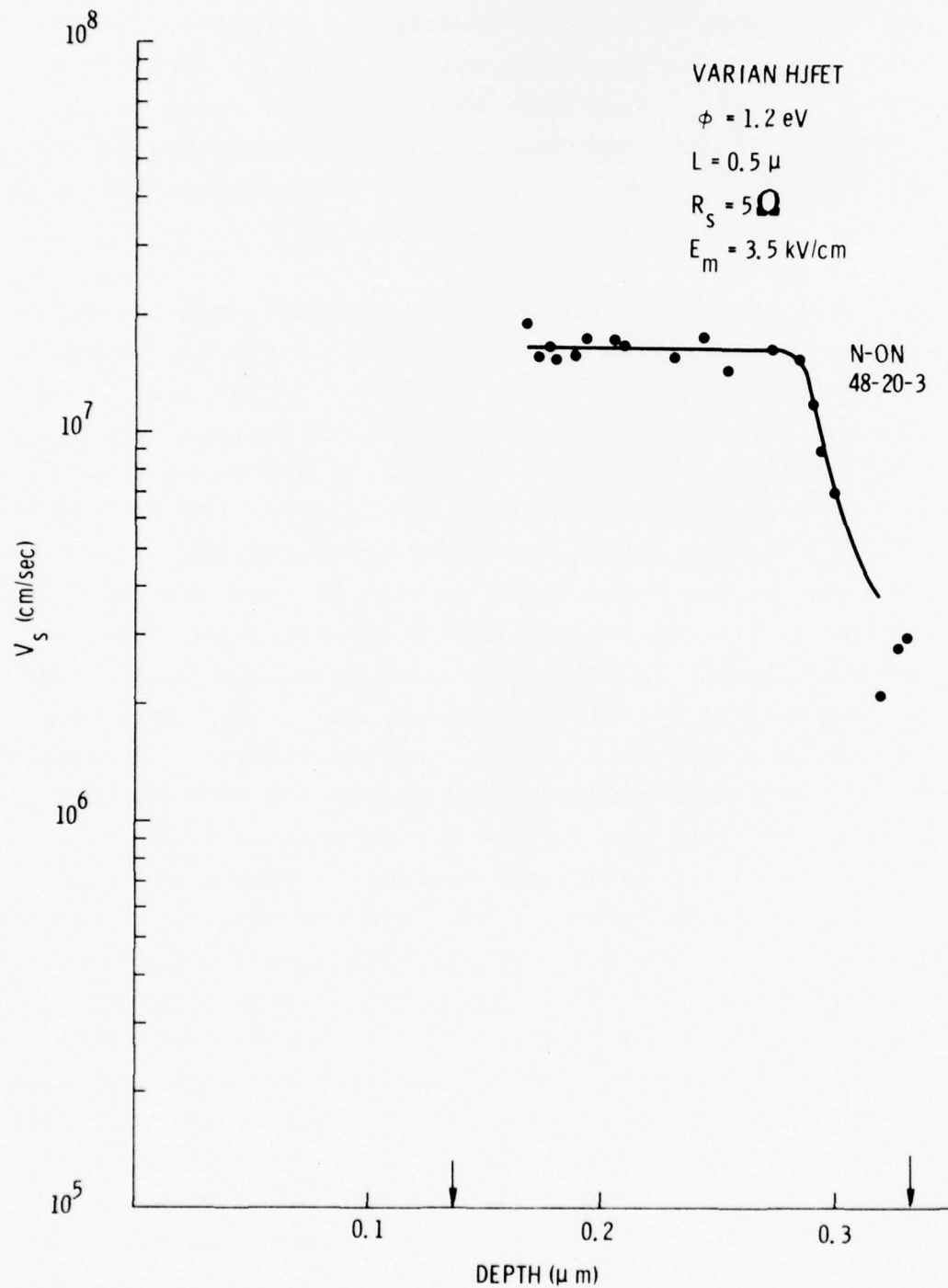


Fig. 23. Velocity profile of the electrons in the channel of a N-ON HJFET.

Table I. S-parameters of a N-ON HJFET in a frequency range of 2-14 GHz at $V_D = +3.3$ V and $V_G = -1$ V.

VARIAN H-FET

(#48-20-3)

$$V_D = 3.3 \quad V_G = -1$$

<u>FREQ</u> <u>(MHz)</u>	S_{11}		S_{21}		S_{12}		S_{22}	
	<u>MAG</u>	<u>ANG</u>	<u>MAG</u>	<u>ANG</u>	<u>MAG</u>	<u>ANG</u>	<u>MAG</u>	<u>ANG</u>
2000.000	.929	-36	1.691	147	.027	71	.849	-9
3000.000	.868	-56	1.615	131	.036	63	.846	-14
4000.000	.808	-75	1.539	116	.041	57	.847	-18
5000.000	.701	-100	1.387	100	.040	51	.816	-22
6000.000	.583	-92	1.308	98	.046	53	.794	-28
7000.000	.635	-120	1.292	83	.042	51	.787	-35
8000.000	.641	-136	1.213	73	.039	51	.813	-40
9000.000	.570	-149	1.127	63	.039	65	.849	-45
10000.000	.541	-159	.991	58	.039	70	.848	-51
11000.000	.663	-170	1.047	48	.037	71	.813	-53
12000.000	.520	153	.938	26	.040	72	.895	-76
13000.000	.450	147	.883	22	.026	88	.698	-83
14000.000	.417	116	1.114	5	.028	65	.730	-81

Table II. Y-parameters of the same HJFET
at the same operating point.

VARIAN H-FET

(#48-20-3)

$$V_D = 3.3 \quad V_G = -1$$

FREQ (MHz)	Y_{11}		Y_{21}		Y_{12}		Y_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000.000	6.300	83	19.870	-12	.318	-88	2.024	42
3000.000	10.345	81	21.113	-18	.471	-85	2.528	55
4000.000	14.865	78	23.010	-24	.616	-83	3.019	64
5000.000	22.553	70	27.058	-33	.771	-82	3.838	66
6000.000	19.650	61	25.610	-39	.897	-85	4.934	68
7000.000	31.126	62	33.407	-43	1.081	-75	6.106	72
8000.000	41.545	57	39.080	-50	1.249	-72	7.009	78
9000.000	48.961	41	43.114	-67	1.498	-65	8.002	83
10000.00	54.040	30	42.774	-77	1.670	-65	9.210	83
11000.00	84.935	23	66.658	-90	2.339	-66	9.687	84
12000.00	49.116	-30	42.172	-140	1.820	-94	16.216	87

Table III. Gain parameters of the same FET
at the same operating point.

VARIAN H-FET
(#48-20-3)

$V_D = 3.3$ $V_G = -1$

<u>FREQ</u> <u>(MHz)</u>	<u>GA MAX</u> <u>(DB)</u>	<u>GU MAX</u> <u>(DB)</u>	<u>S₂₁</u> <u>(DB)</u>	<u>S₁₂</u> <u>(DB)</u>	<u>K</u> <u>(MAG)</u>	<u>V</u> <u>(MAG)</u>
2000.000		18.75	4.56	-31.37	.54	.95
3000.000		15.70	4.17	-28.87	.70	.61
4000.000		13.83	3.75	-27.70	.85	.44
5000.000	11.04	10.53	2.84	-28.07	1.56	.18
6000.000	8.70	8.46	2.34	-26.78	2.06	.11
7000.000	9.27	8.67	2.23	-27.57	1.96	.12
8000.000	9.53	8.67	1.68	-28.23	1.89	.12
9000.000	9.49	8.29	1.04	-28.14	1.77	.11
10000.00	7.93	6.94	-.08	-28.25	2.19	.09
11000.00	8.90	7.62	.40	-28.70	1.97	.11
12000.00	9.47	7.82	-.56	-27.86	1.50	.12

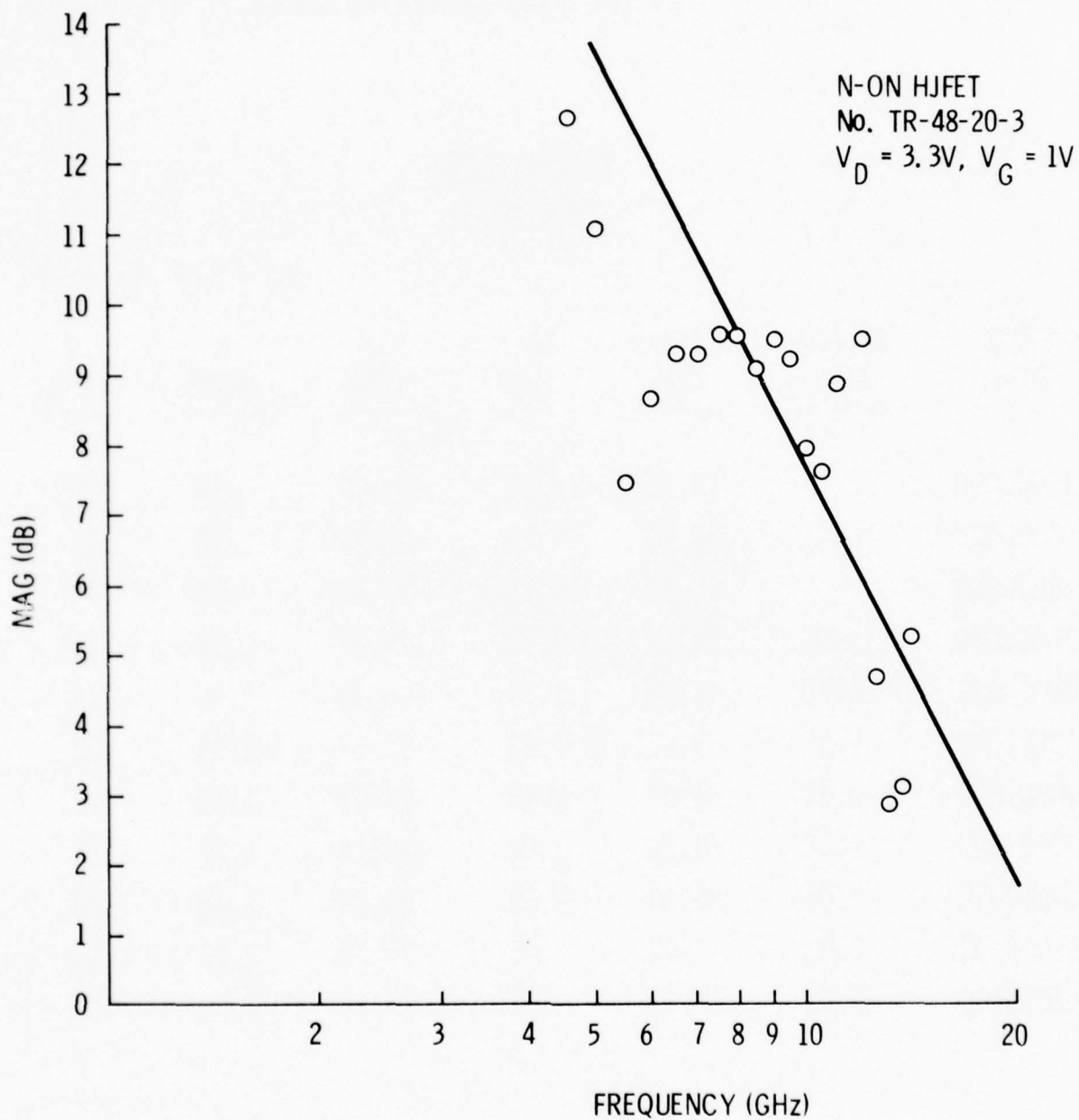


Fig. 24. MAG vs frequency for the above HJFET. The solid line denotes the fitted 6 dB/octave line.

NAME TR-48-20-3	TITLE $V_D = 3.3V$, $V_G = -1V$	DWG NO Varian H-FET
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY PINE BROOK N.J. © 1966 PRINTED IN USA	DATE January 1977

IMPEDANCE OR ADMITTANCE COORDINATES

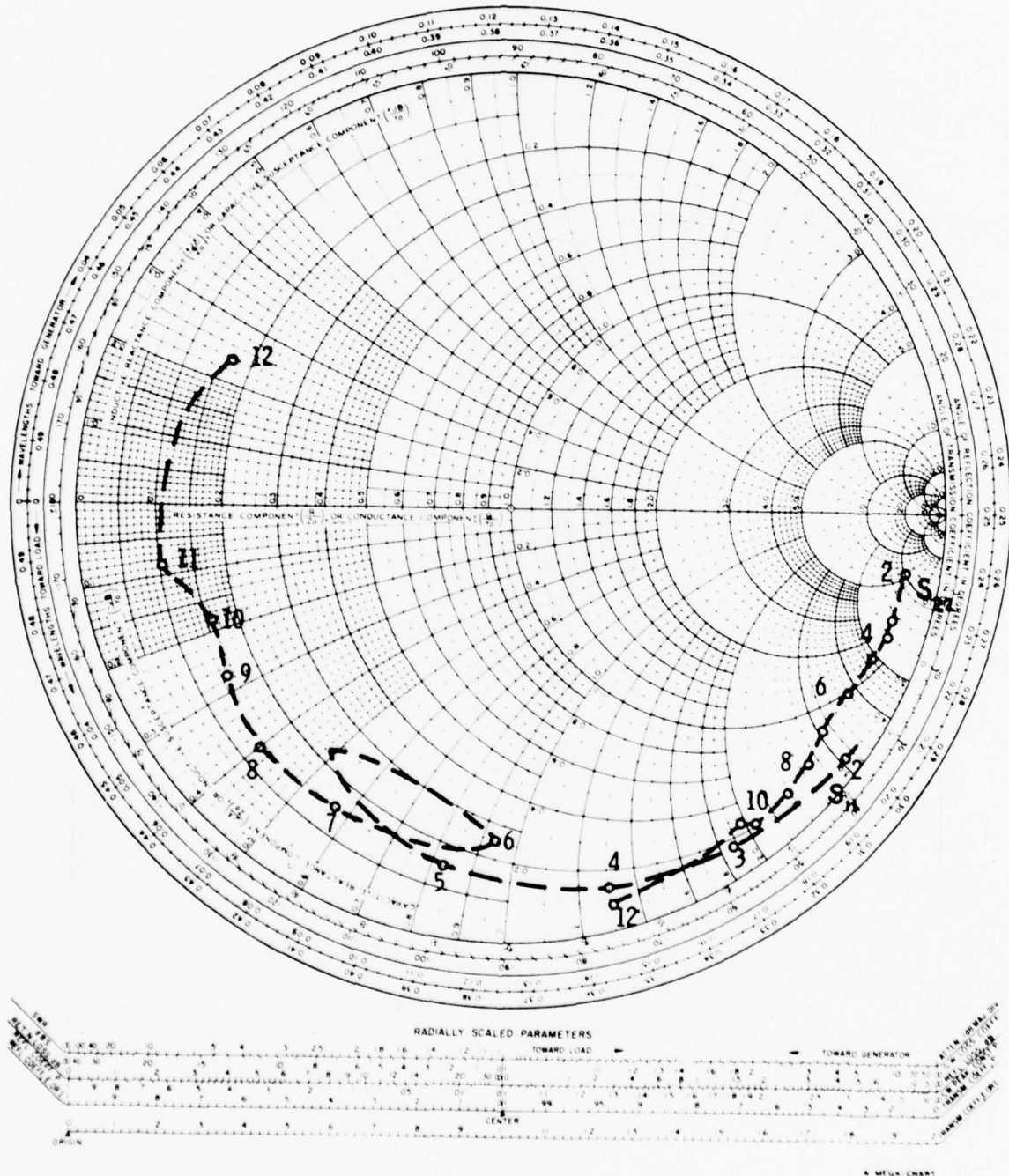


Fig. 25. S_{11} and S_{22} parameters associated with a N-ON HJFET. Looping in S_{11} is attributed to calibration errors.

VARIAN H-FET
EQUIVALENT CKT
 $L_g \approx 0.5 \mu m$
 $Z = 300 \mu m$

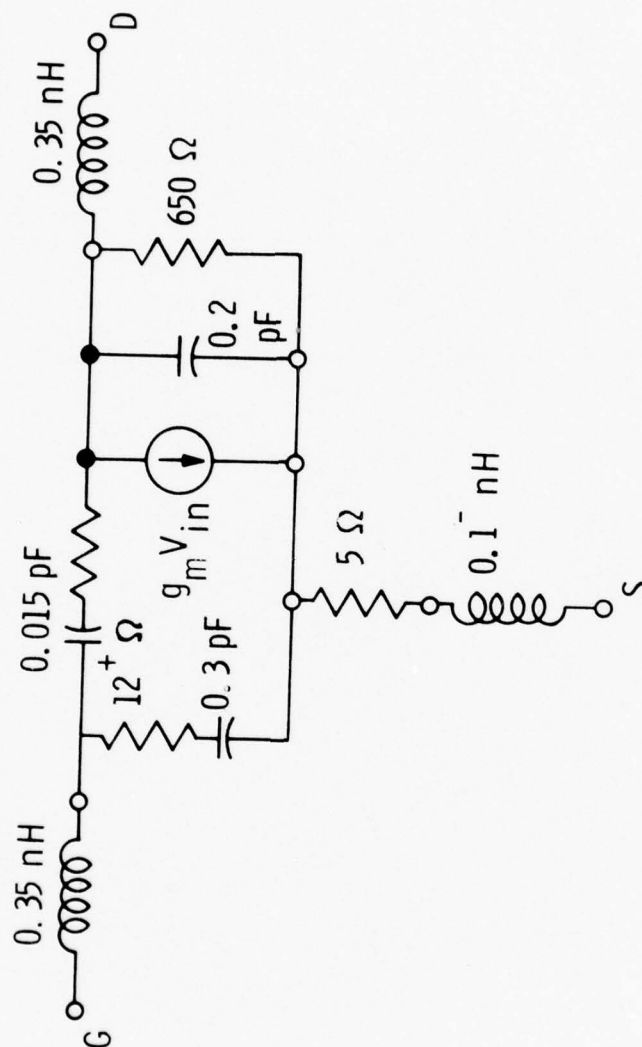


Fig. 26. Equivalent circuit model associated with a N-ON HJFET calculated from the measured S-parameters.

a quick means of checking for stability is to see if $K > 1$, this does not necessarily guarantee absolute stability even with passive input and output loads. The device is stable for any passive load and/or source if

$$a. \quad |s_{11}| < 1, |s_{22}| < 1, K > 1$$

$$b. \quad \left| \frac{|s_{12} s_{21}| - |M^*|}{|s_{11}|^2 - |D|^2} \right| > 1$$

$$c. \quad \left| \frac{|s_{12} s_{21}| - |N^*|}{|s_{22}|^2 - |D|^2} \right| > 1$$

where

$$D = |s_{11} s_{22} - s_{12} s_{21}|$$

$$M = s_{11} - D s_{22}^*$$

$$N = s_{22} - D s_{11}^*$$

or

$$a. \quad K > 1$$

$$b. \quad 1 + |s_{11}|^2 - |s_{22}|^2 - |s_{11}| |s_{22} - s_{12} s_{21}|^2 > 0$$

Either one of the above conditions is satisfied by the N-ON HJFETs tested at 8 GHz, which means that no passive source and/or load can make the device unstable.

Large-signal input reflection and transmission switching measurements were carried out in a 50-ohm line microstrip circuit. For this purpose, a pulse having a rise time of about 5 ns is

used after the rise time is improved to 200 ps with the aid of a step recovery diode (SRD). The pulse shapes before and after this improvement are shown in Fig. 27 along with the circuit used. Figure 28(a) shows the actual circuit realized on an Al_2O_3 substrate and 28(b) illustrates its MIC diagram. With the aid of a sampling oscilloscope, the reflected pulse from the gate in the reflection configuration (Fig. 29) and the transmitted pulse in the transmission configuration (Fig. 30) were compared to a reference pulse to determine the rise time increment of the input pulse and the delay time. A photograph of the output biasing circuit and its MIC diagram are shown in Fig. 28(c) and 28(d) respectively.

Knowing the input capacitance charging time, the actual gate voltage for the incident voltage can be obtained. The output response to the actual gate voltage is then calculated using the drain characteristic of the HJFET assuming zero delay. Finally, the zero delay output is compared with the actual output response in the transmission configuration to find the propagation delay of the device as shown in Fig. 31. For a positive input pulse of 300 mV, the intrinsic propagation delay time is about 20 ps and the input capacitance charging time is about 20 ps. The drain load has been chosen to be 100 ohms.

2.4.4 Normally-Off HJFET Device Results

The drain I-V characteristic of a N-OFF HJFET is illustrated in Fig. 32. The dc extrinsic transconductance increases with the applied gate bias as shown in Fig. 33 along with the drain saturation current. At $V_G = +3.0$ V, the extrinsic dc transconductance (g_m) for a 300-micron gate periphery approaches 90 mmhos. The intrinsic transconductance (g_m^i) at the same bias is about 1000 mmhos. This is clearly due to the hole injection into the channel since at $V_G = +3$ V both the gate-source and

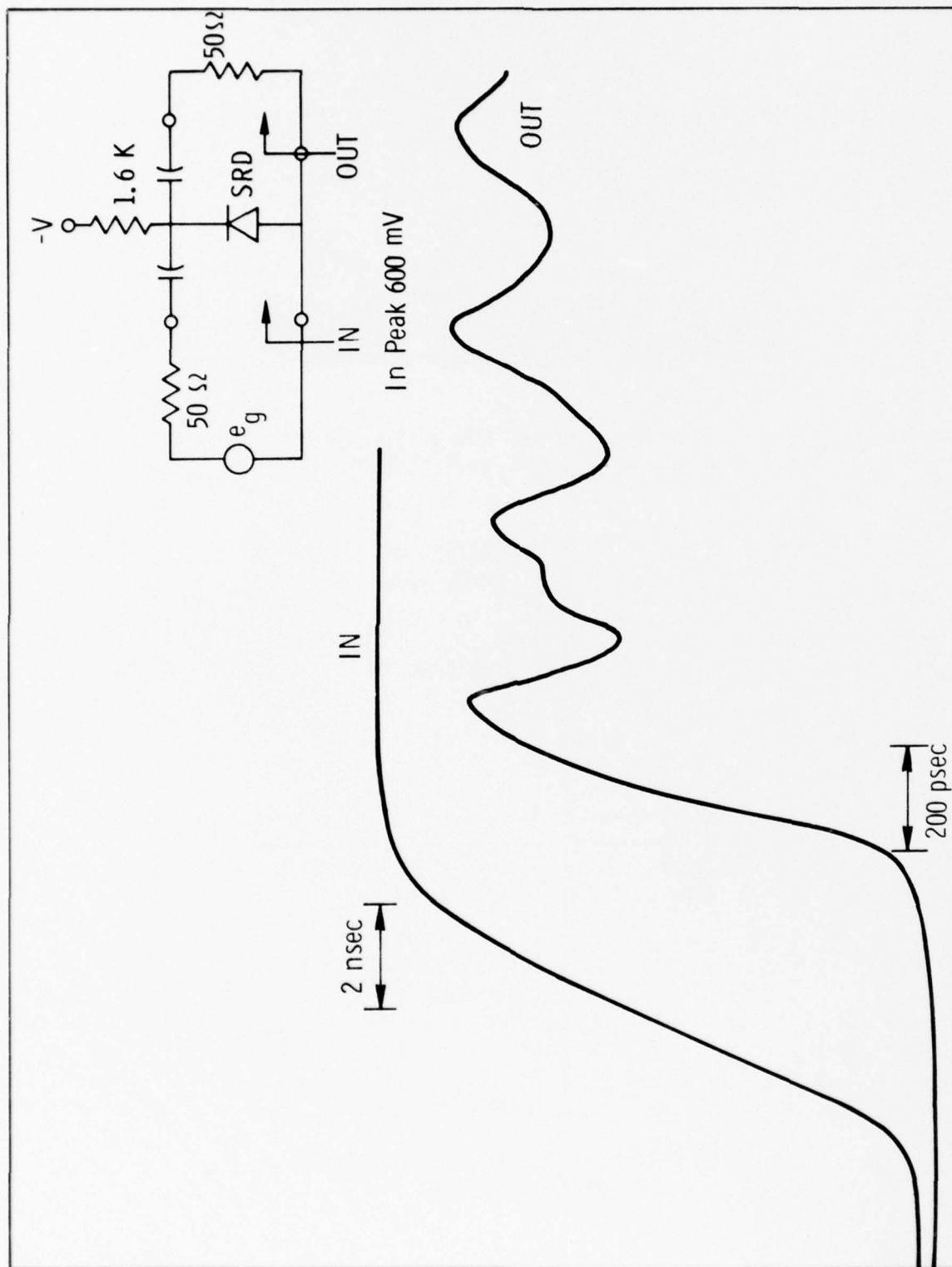


Fig. 27. The input pulse and the output pulse of a step recovery diode circuit used to improve the pulse rise time from 5 ns to 200 ps. A second stage can reduce the rise time to about 60 ps.

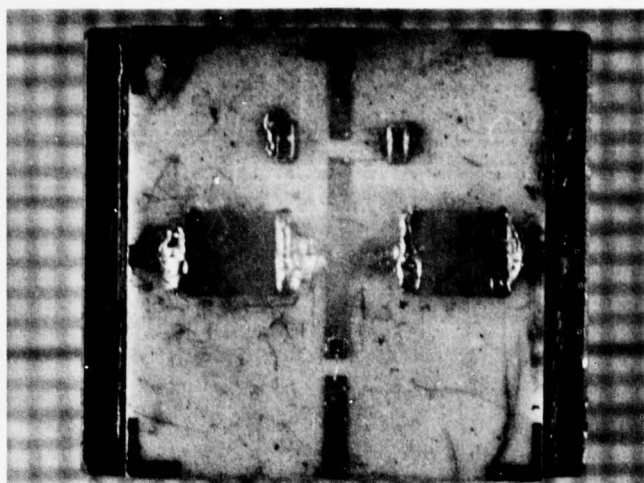
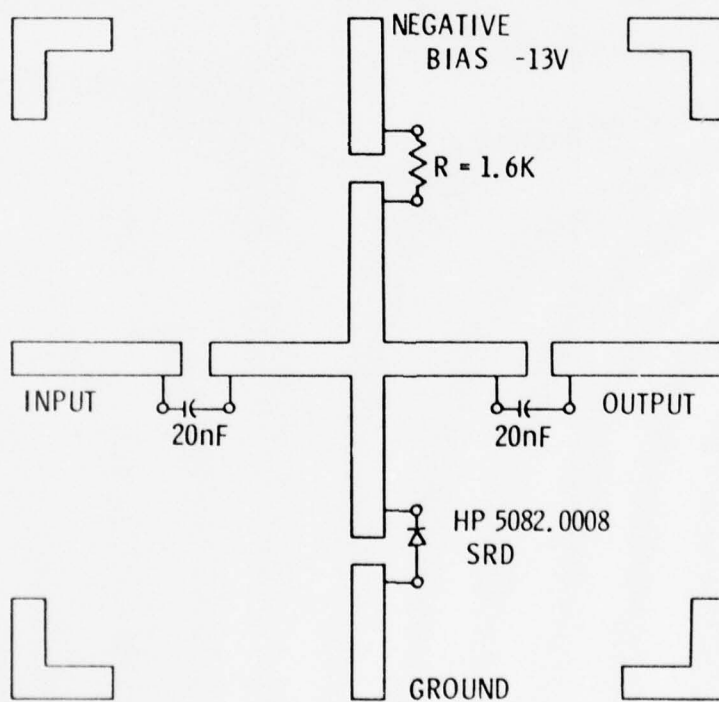


Fig. 28(a). Photograph of the pulse improvement circuit realized on a Al_2O_3 substrate.



INPUT PULSE SHARPENING CIRCUIT USING
STEP RECOVERY DIODES

Fig. 28(b). Schematic MIC diagram of the same circuit in (a).

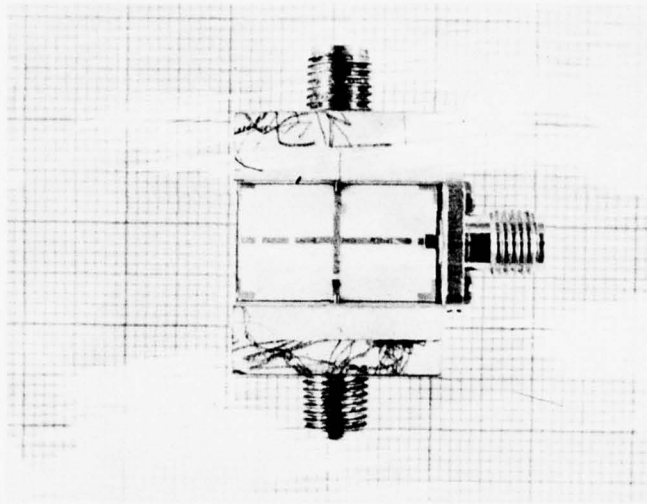


Fig. 28(c). Photograph of the output circuit used to carry out large-signal switching measurements.

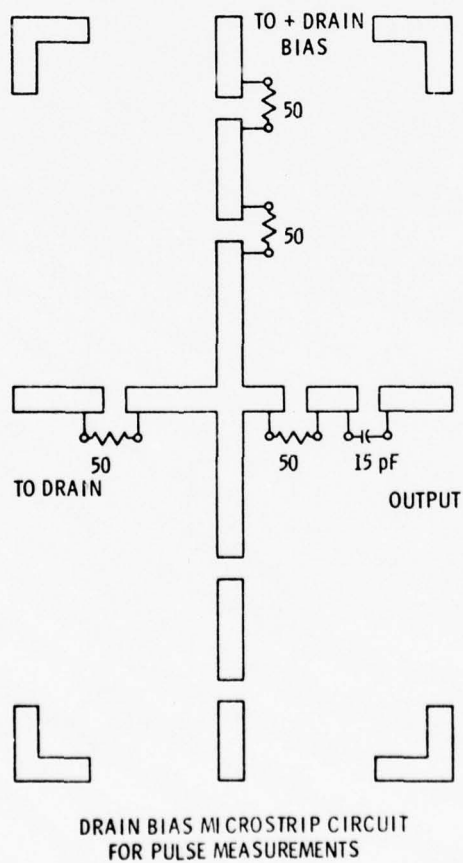
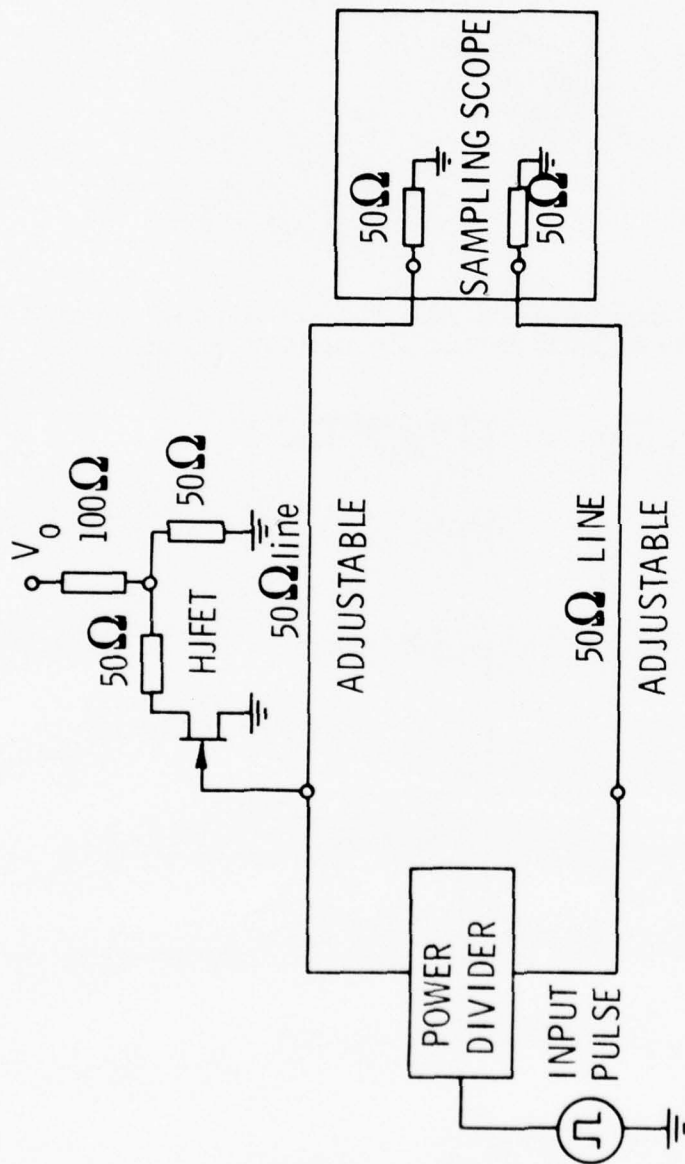
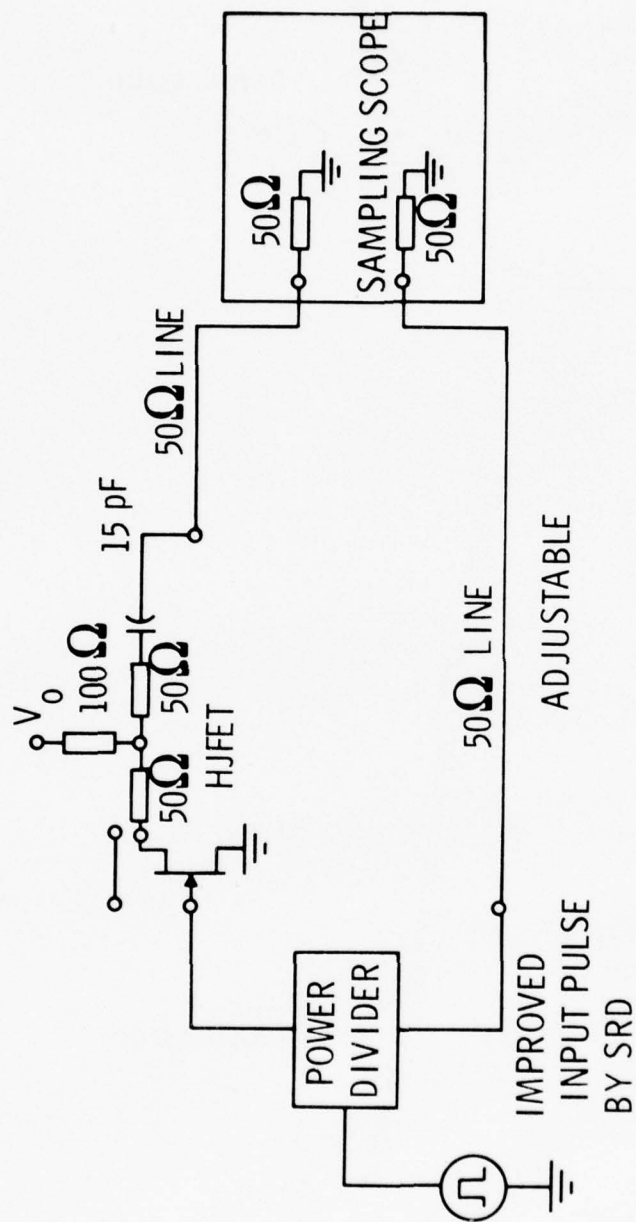


Fig. 28(d). Schematic MIC configuration of the same circuit in (c).



INPUT CAPACITANCE CHARGING TIME MEASUREMENT SETUP

Fig. 29. Reflection configuration for measuring the input capacitance charging time.



INTERNAL SIGNAL DELAY MEASUREMENT SETUP

Fig. 30. Transmission configuration for measuring the delay time.

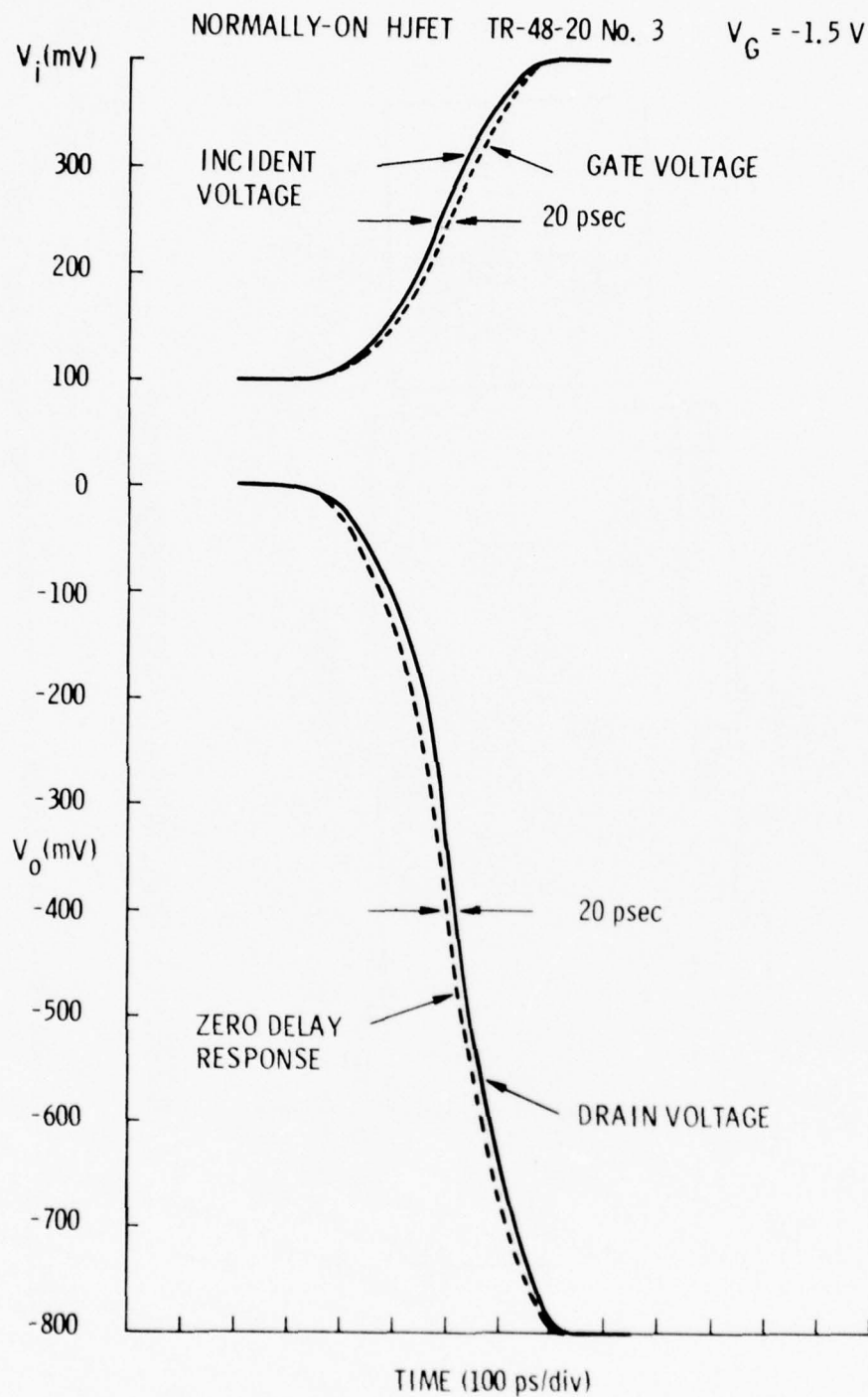


Fig. 31. Large signal switching response of a N-ON HJFET biased at $V_G = 1.5 \text{ V}$ and $V_D = +3 \text{ V}$ to a positive gate pulse. The propagation delay time is about 20 ps.

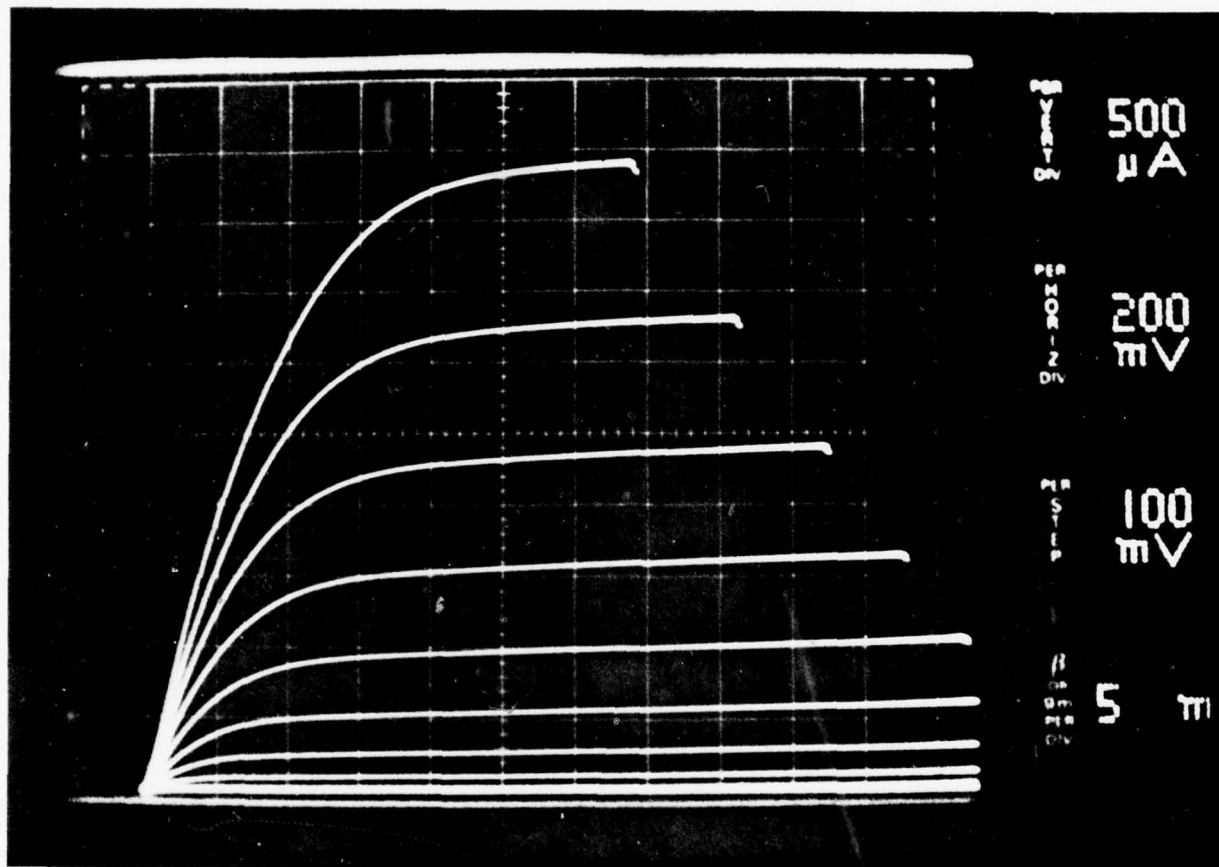


Fig. 32. Drain I-V characteristics of a N-OFF HJFET having a gate bias of up to +0.9 V in 0.1 V increments. The gate length is estimated to be about 0.6 micron with an associated periphery of about 300 microns.

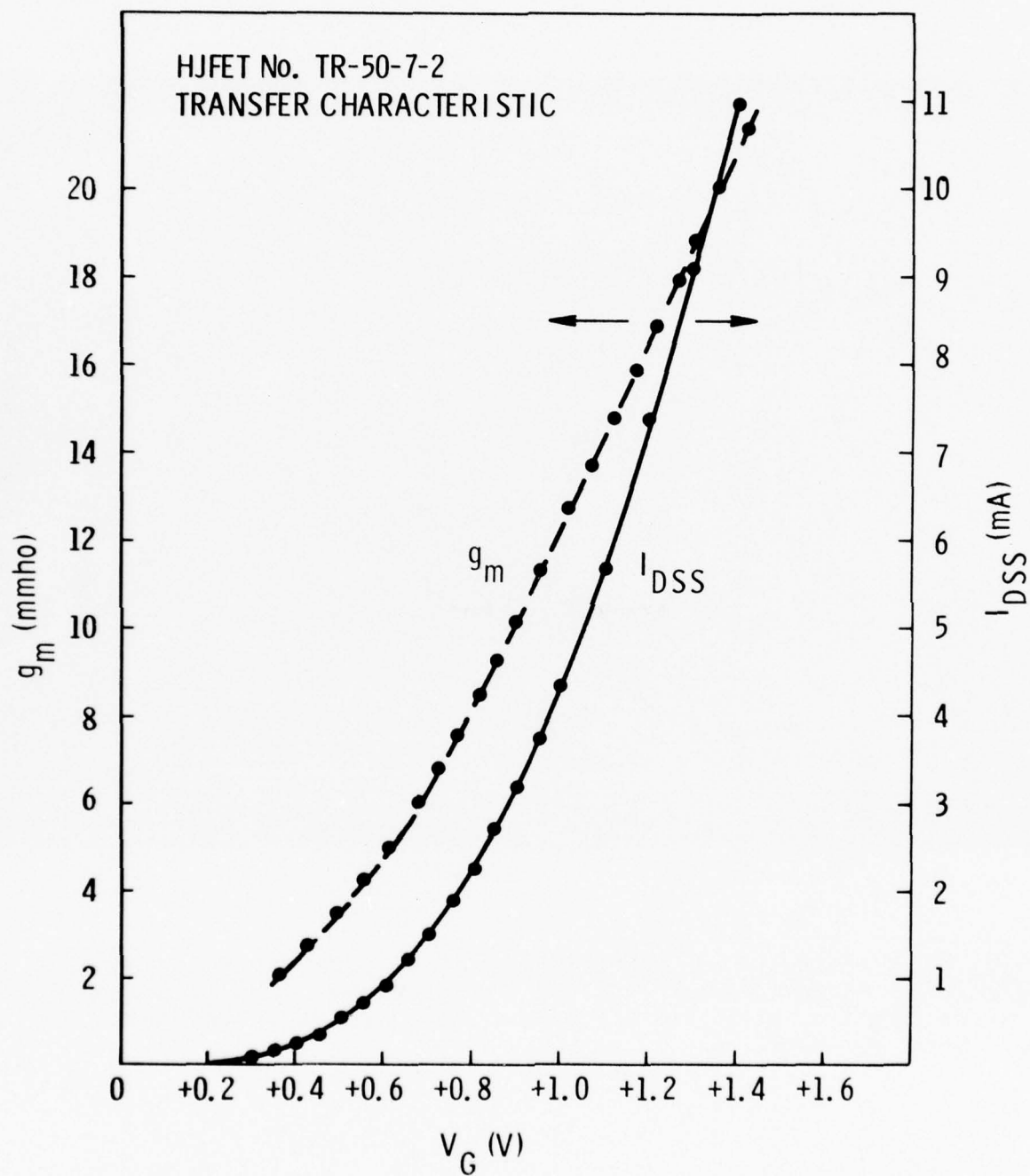


Fig. 33. The drain saturation current and the extrinsic dc transconductance of a N-OFF HJFET as a function of the gate bias.

the gate-drain diodes are heavily forward biased. The typical source resistance (R_S) and drain resistance (R_D) of the N-OFF HJFETs are both about 23 ohms and 6 ohms for $V_G = +0.5$ and $+1.0$ V respectively, determined by a technique described by Giacoletto.⁵ The gate resistance (R_G) on the other hand is about 15 ohms.

As described earlier, the velocity of electrons as a function of depth into the channel layer was calculated using the slope of I_{DS} vs $\sqrt{V_{eff}}$, as shown in the Appendix. However, this technique does not hold for devices with small pinch-off voltages (V_P) such as N-OFF HJFETs (i.e. $3 E_M L_g / V_P \geq 1$), and the velocity does not reach the saturation value according to Turner and Wilson.⁶ Therefore, other means should be used to calculate the saturation velocity in the thin active layers ($\sim 1400 \text{ \AA}$) used for N-OFF HJFETs. We have shown the drain current $v_s \sqrt{V_{eff}}$ in Fig. 34 where the properties of the N-OFF devices are deduced from the measurements on the N-ON HJFETs since the epitaxial channel layers were grown under equivalent conditions. On the right, the solid line represents the measured I_{DS} as a function of the square root of the effective gate bias ($\sqrt{V_{eff}}$), which is linearly related to the depth for a N-ON device. On the other hand, the slope of this curve is proportional to the velocity in the channel. (Notice that near the interface velocity degradation takes place.) If there were no velocity degradation, the drain current would have been given by the dashed line whose slope is equal to that of the solid line away from the interface.

Since the velocity in the channel of a N-OFF HJFET does not reach the saturation value, a direct deduction of the velocity from the N-OFF drain current analogous to the N-ON case does not hold. But the velocity can be deduced from the data associated with the N-ON devices, because the only difference between the two types of devices is the thickness of the channel

layer. Let us for a moment assume that the velocity in the channel of a N-OFF HJFET reaches saturation and there is no velocity degradation near the substrate interface. The I_{DS} associated with such a device with $V_p = 1.4$ V would have been represented by the dashed line on the left, whose slope is equal to that for the N-ON case. However, with the velocity degradation observed from the N-ON device, the I_{DS} is given by the solid curve to the left of the dashed curve. Since velocity saturation does not take place, I_{DS} is bound to be smaller than indicated by the solid line, as observed in the experimental devices. Using Turner and Wilson's theory, the u value (solution to the polynomial in Ref. 6, Eq. (7)) is calculated by multiplying the solid line by $(1-u)$. These values of I_{DS} designated by " v_s " in Fig. 34 are in quite good agreement with the experimental results. Shown in Fig. 35 are the velocity profiles in the channels of N-ON (right) and the N-OFF (left) HJFETs as a function of depth into the layer calculated from Fig. 34 as described in the Appendix. As can be seen, about 500 \AA of the channel layer near the substrate shows velocity degradation and v_s away from this interface appears to be about $1.7 \times 10^7 \text{ cm/sec}$. The Solid curve on the left is calculated using the curve for N-OFF HJFET in Fig. 34 marked " v_s " which is really what is expected, but one should remember that v_s is not reached in the N-OFF channel. The square and the triangle data points in Fig. 35 correspond to two different N-OFF HJFETs under the assumption that carrier velocity saturation does take place and there is no injection from the gate into the channel (which as we have seen, is not strictly true in practice). It is therefore very clear that the presence of a bad interface results in velocity degradation near the interface. The N-ON FETs (except when biased for low noise) are not affected by this velocity degradation as much as the N-OFF devices. In the case of N-OFF FETs, the channel itself is completely depleted by the built-in potential so that any drain current flow is the result of opening of the channel

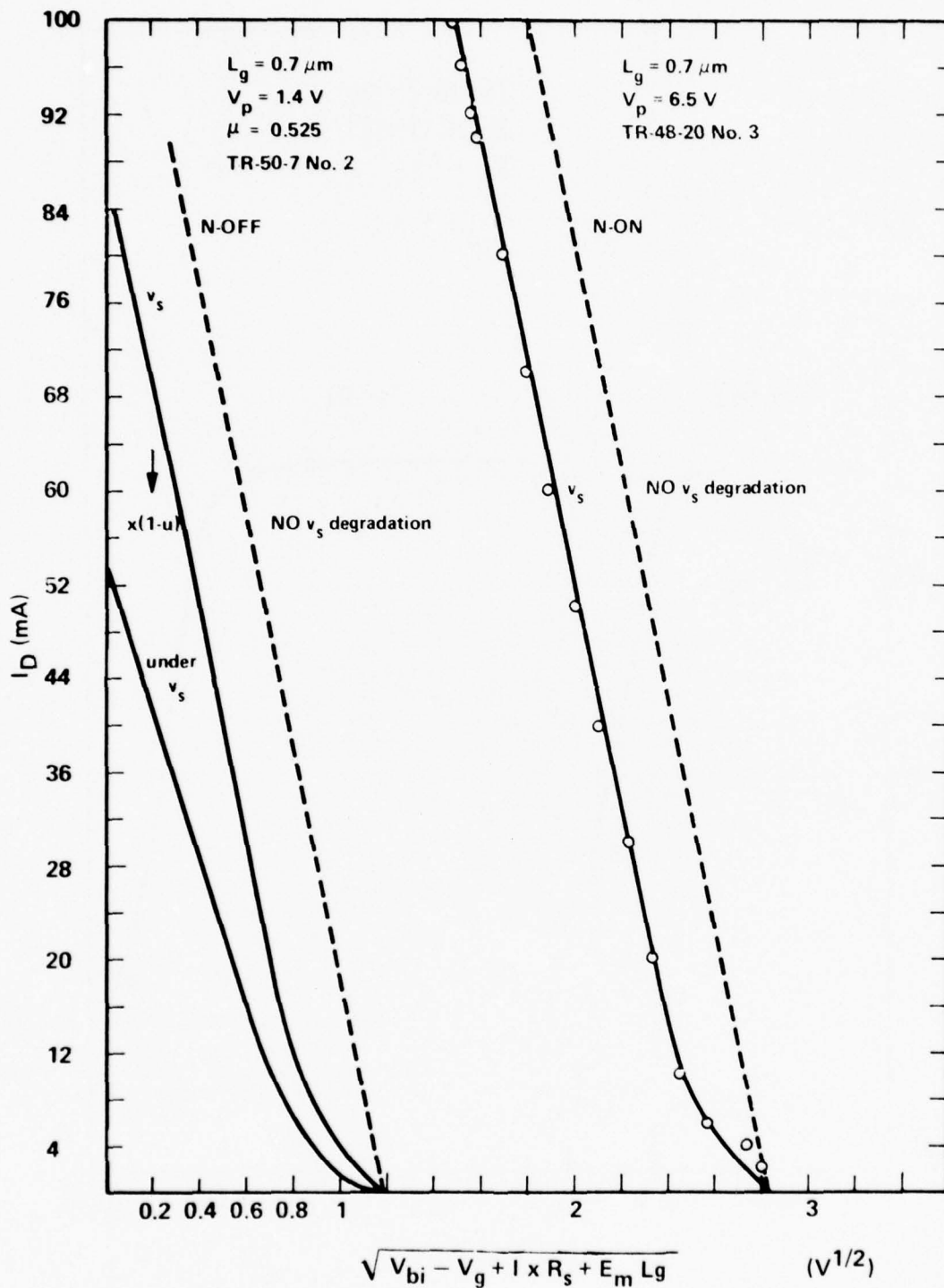


Fig. 34. Drain current vs the square root of the effective gate bias with (solid lines) and without (broken lines) velocity degradation for a N-ON (right) and for a N-OFF HJFET deduced from the N-ON device data (left).

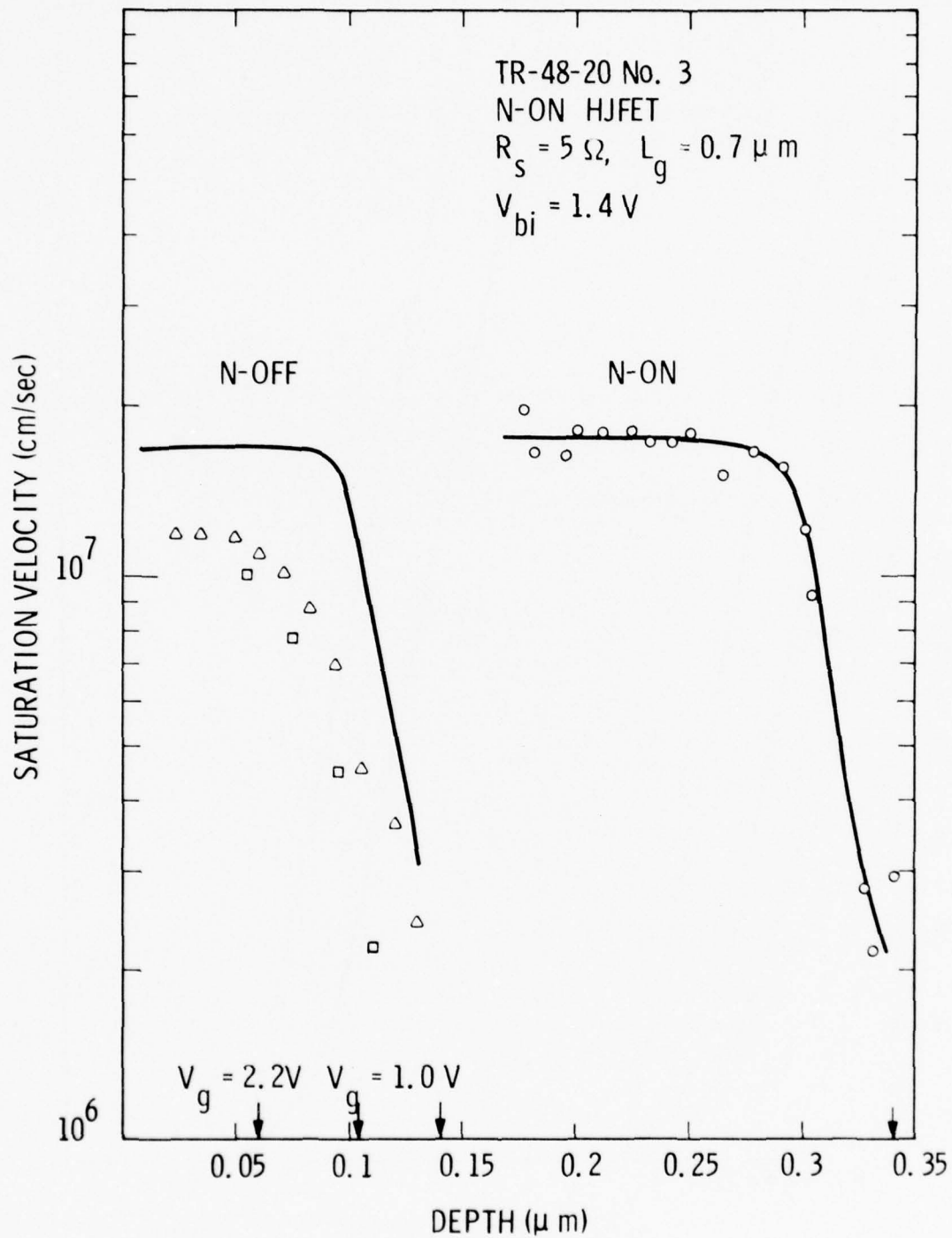


Fig. 35. Velocity profile in the active layer of a N-ON HJFET (right) and of a N-OFF HJFET (left) deduced from the N-ON data.

by the applied positive gate bias. With Schottky-barrier N-OFF FETs, this positive gate bias is limited to 0.5 V due to excessive forward gate current; therefore only the velocity degraded part of the channel can be opened for the current transport, which limits the performance. However, having the heterojunction gate enables one to apply up to +1.2 V gate bias to utilize more of the channel having the higher velocity. This can result in faster device performance.

Small signal S-parameter measurements covering a range of 2-12 GHz were made similar to N-ON devices and the results are tabulated in Tables IV, V, and VI. Devices having about 0.6-micron gates exhibited a MAG of about 9 dB at 2 GHz with a fall-off of slightly more than 6 dB/octave, as shown in Fig. 36. This faster roll-off is attributed to possible calibration errors in the automatic network analyzer and/or to the feedback capacitance. S-parameters of a device operating at a drain bias of $V_D = +2.0$ V and the gate bias of $V_G = +0.5$ V are shown on the Smith chart in Fig. 37 along with the S_{21} for $V_G = +1.0$ V.

One can see that the S-parameters associated with a N-OFF device show marked differences from the N-ON devices in term of S_{11} and S_{21} . Notice that S_{11} falls rapidly with frequency, indicating a large input capacitance (0.4 pF at $V_G = +0.5$ V and 0.77 pF at $V_G = +1.0$ V). S_{21} is small and also falls rapidly with frequency. S_{21} for $V_G = +1.0$ V is quite large and even though the larger associated input capacitance offsets some of this increase, the overall gain is larger than for $V_G = +0.5$ V. Figure 38 shows the equivalent circuit for this N-OFF HJFET for both $V_G = +0.5$ and 1.0 V, calculated as described for the N-ON devices.

Large-signal switching properties have been measured in the same way as for the N-ON HJFET case. Figure 39 shows the input incident pulse, actual gate pulse, zero delay response

Table IV. S-parameters of a N-OFF HJFET in a frequency range of 2-12 GHz at $V_D = +2$ V and $V_G = +1$ V.

VARIAN HJFET
NORMALLY-OFF
(#TR50-7-6)

$V_D = 2V$ $V_G = + 1.0V$

FREQ. (MHz)	S_{11}		S_{21}		S_{12}		S_{22}	
	MAG	ANG	MAG	ANG	MAG	ANG	MAG	ANG
2000.000	.725	-39	1.192	128	.048	57	.831	-13
3000.000	.596	-52	1.034	110	.061	49	.797	-19
4000.000	.498	-63	.924	96	.068	44	.796	-23
5000.000	.385	-72	.821	83	.073	40	.770	-27
6000.000	.302	-82	.756	71	.077	37	.739	-34
7000.000	.247	-88	.701	61	.078	35	.717	-43
8000.000	.205	-93	.615	50	.072	32	.701	-50
9000.000	.151	-97	.569	44	.074	33	.723	-55
10000.00	.111	-96	.534	36	.075	31	.734	-61
11000.00	.090	-91	.485	24	.070	26	.658	-67
12000.00	.033	-93	.445	15	.059	26	.570	-70

Table V. Y-parameters of the same device
at the same operating point.

VARIAN H-FET
NORMALLY-OFF
(#TR50-7-6)

$$V_D = 2V \quad V_G = + 1.0V$$

<u>FREQ</u> <u>(MHz)</u>	<u>Y₁₁</u>		<u>Y₂₁</u>		<u>Y₁₂</u>		<u>Y₂₂</u>	
	<u>MAG</u>	<u>ANG</u>	<u>MAG</u>	<u>ANG</u>	<u>MAG</u>	<u>ANG</u>	<u>MAG</u>	<u>ANG</u>
2000.000	7.356	64	15.836	-30	.639	-102	2.603	54
3000.000	10.429	58	15.776	-43	.925	-104	3.579	60
4000.000	13.038	52	15.669	-54	1.147	-105	4.365	66
5000.000	15.568	43	15.778	-67	1.405	-109	5.295	67
6000.000	17.854	36	16.322	-77	1.663	-111	6.784	67
7000.000	19.229	31	16.554	-86	1.849	-112	8.734	69
8000.000	20.181	26	15.538	-97	1.824	-114	10.182	60
9000.000	20.551	20	14.807	-103	1.919	-114	11.158	71
10000.000	20.392	16	14.253	-111	1.997	-115	12.525	73
11000.000	20.280	13	13.923	-123	2.013	-122	14.270	67
12000.000	20.408	6	13.706	-138	1.805	-127	15.271	59

Table VI. Gain parameters of the same
FET at the same bias point.

VARIAN HJFET
NORMALLY-OFF
(#TR50-7-6)

$$V_D = 2V \quad V_G = + 1.0V$$

<u>FREQ.</u> <u>(MHz)</u>	<u>GA MAX</u> <u>DB</u>	<u>GU MAX</u> <u>DB</u>	<u>S₂₁</u> <u>DB</u>	<u>S₁₂</u> <u>DB</u>	<u>K</u> <u>MAG</u>	<u>U</u> <u>MAG</u>
2000.000	9.28	9.86	1.52	-26.35	1.63	.24
3000.000	6.08	6.56	.29	-24.35	2.22	.13
4000.000	4.52	4.90	-.69	-23.40	2.52	.09
5000.000	2.64	2.88	-1.71	-22.72	3.14	.05
6000.000	1.26	1.40	-2.44	-22.27	3.74	.03
7000.000	.23	.32	-3.09	-22.13	4.31	.02
8000.000	-1.16	-1.10	-4.23	-22.84	5.61	.01
9000.000	-1.61	-1.58	-4.89	-22.64	5.64	.01
10000.00	-2.05	-2.03	-5.44	-22.51	5.77	.01
11000.00	-3.80	-3.78	-6.28	-23.08	8.33	.00
12000.00	-5.33	-5.33	-7.04	-24.65	12.98	.00

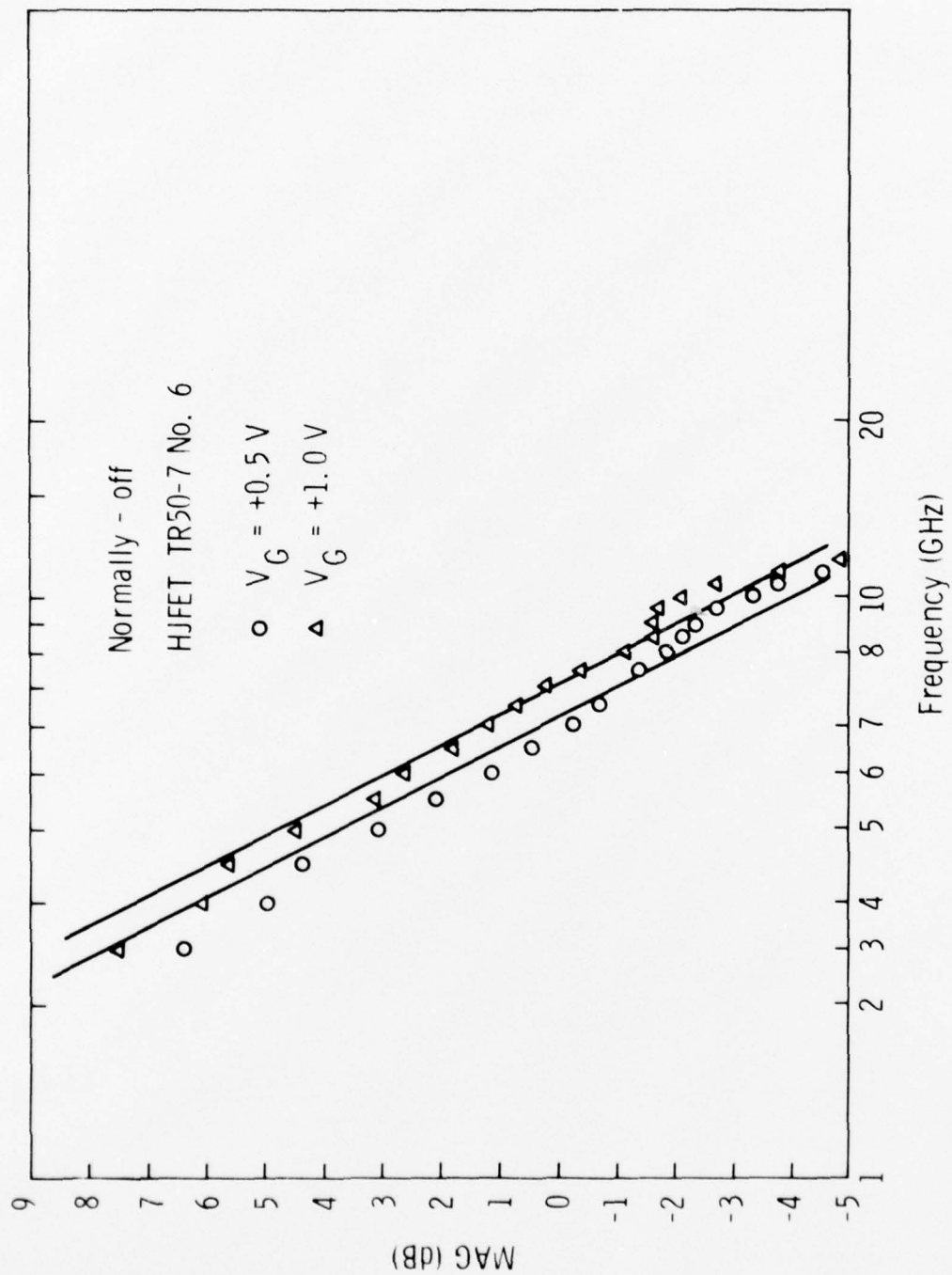
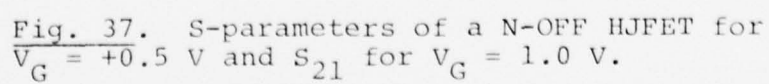


Fig. 36. MAG vs frequency for a N-OFF HJFET at a gate bias of +0.5 V and +1.0 V.

IMPEDANCE OR ADMITTANCE COORDINATES

HJFET
No. 50-7-4
 $V_D = 2V$

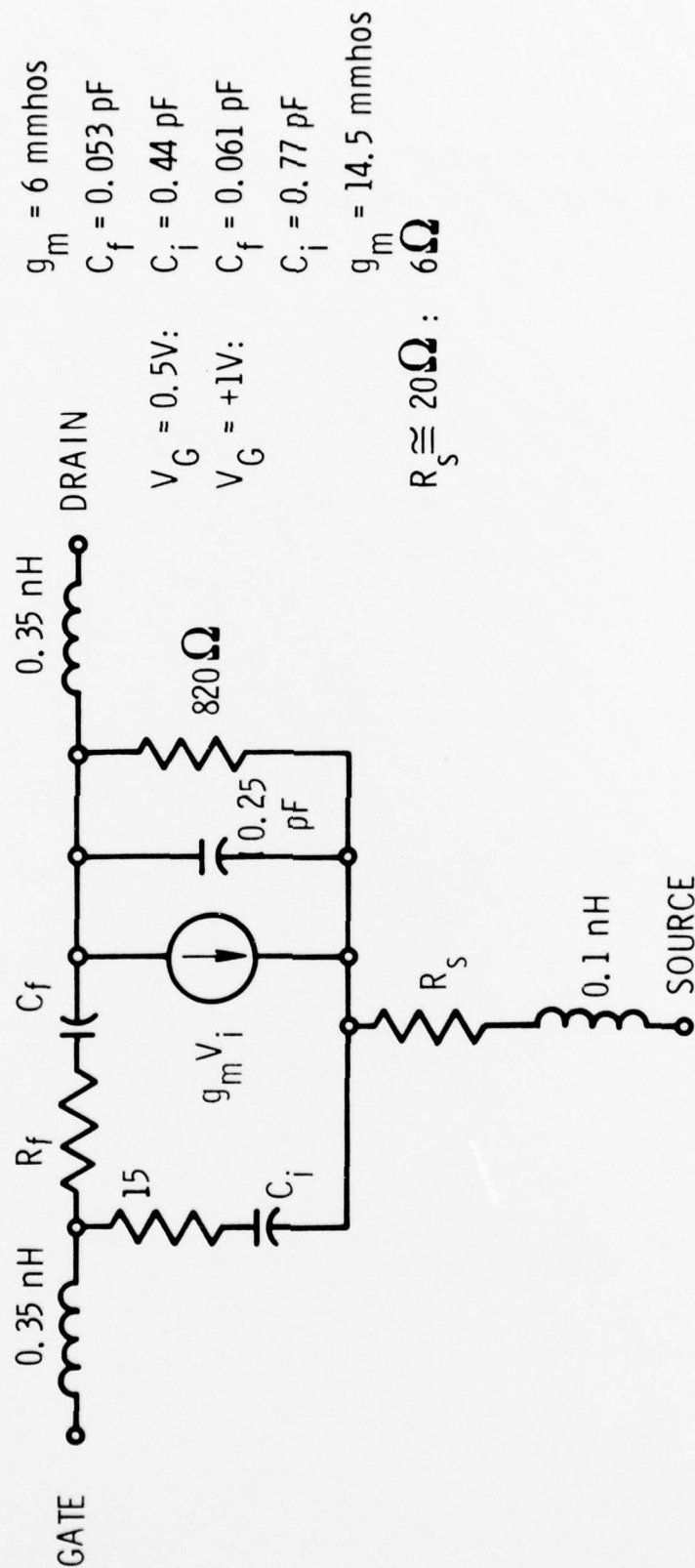


Fig. 38. Equivalent circuit for a N-OFF HJFET biased at $V_D = 2 \text{ V}$, and $V_G = 0.5 \text{ V}$ and $V_G = +1 \text{ V}$ where $g_m = 6 \text{ mmhos}$, $C_f = 0.05 \text{ pF}$, $C_i = 0.44 \text{ pF}$, and $R_s \approx 20 \text{ ohms}$ corresponding to $V_G = +0.5 \text{ V}$; and $g_m = 14.5 \text{ mmhos}$, $C_f = 0.061 \text{ pF}$, $C_i = 0.77 \text{ pF}$, and $R_s = 6 \text{ ohms}$ corresponding to $V_G = +1 \text{ V}$.

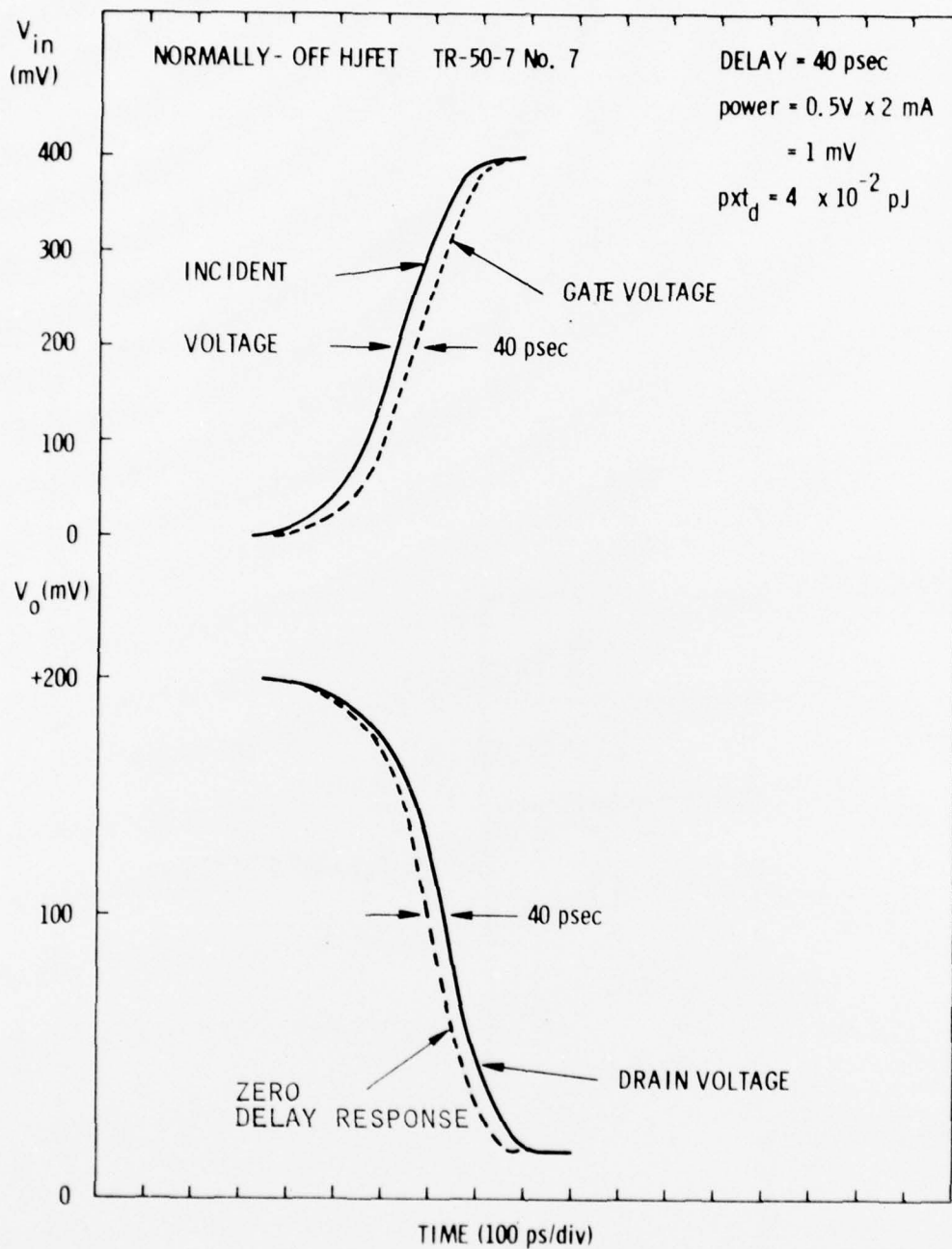


Fig. 39. Large-signal switching response of a N-OFF HJFET to a +400 mV incident gate pulse. The input capacitance charging time and the intrinsic propagation delay time are about 40 ps each.

and the output response. The input capacitance charging time to an incident positive pulse of +400 mV has been measured to be 40 ps. The output pulse is compared to the zero delay response to find the intrinsic propagation delay time which typically is about 40 ps. The arbitrarily chosen drain load is again 100 ohms. This result is remarkable in that the switching time is very short and the associated drain power consumption of 1 mW or less is very small although it is somewhat arbitrary at this point to quote a power consumption. The N-OFF HJFET gate periphery of 300 microns is too long for switching applications owing to the larger power dissipation required (due to the large drain current). By reducing the gate periphery, the drain power dissipation can be reduced. A gate periphery of about 20 microns is about the limit below which stray effects can play a dominant role. The device performance indicates that such a logic circuit would have a clocking speed of about 4 GHz. This coupled with low drain dissipation make N-OFF HJFETs a strong candidate for large-scale integration.

3. RECOMMENDATIONS FOR FURTHER STUDY

The gate resistance must be lowered to 5 ohms or below for a 300-micron wide periphery. This can theoretically be done by increasing the doping in p^+ -GaAs, by using a different dopant such as Mg diffusion or Be ion-implantation. A second approach would be to incorporate a different metal for the gate metallization and AuGe/Ni/Au for the source and drain. The substrate interface degradation must be overcome by possibly growing a high resistivity buffer layer between the active channel layer and the substrate. The p^+ -GaAs layer thickness needs to be lowered to about 0.2 to 0.3 micron for increased device fabrication uniformity. In addition, the minimum affordable thickness of the gate $Al_{0.5}Ga_{0.5}As$ semiconductor should be explored. After these problems have been overcome, a thorough comparative evaluation of HJFETs with competing technologies should be made. The chief interest appears to be development of logic-integrated circuits, utilizing N-OFF HJFETs. Medium-scale integrated circuits, e.g. a ring oscillator, can be fabricated to verify the propagation delay. Possibly an attempt can also be made to fabricate NAND/NOR gates. N-OFF HJFET NAND gates require relatively simple circuitry as opposed to N-ON FETs.

Figure 40 summarizes the performance of high-speed Si and GaAs based logic. It should be noted that the GaAs-based devices are approximately one order of magnitude faster than Si devices. The N-OFF HJFET as a device is also shown as having 40 psec of delay time and about 1 mW of drain power consumption. By improving the device performance which is feasible with the current state-of-the art technology, HJFET logic can potentially have 100-200 ps delay times and with an associated 0.5 to 1.0 mW power consumption.

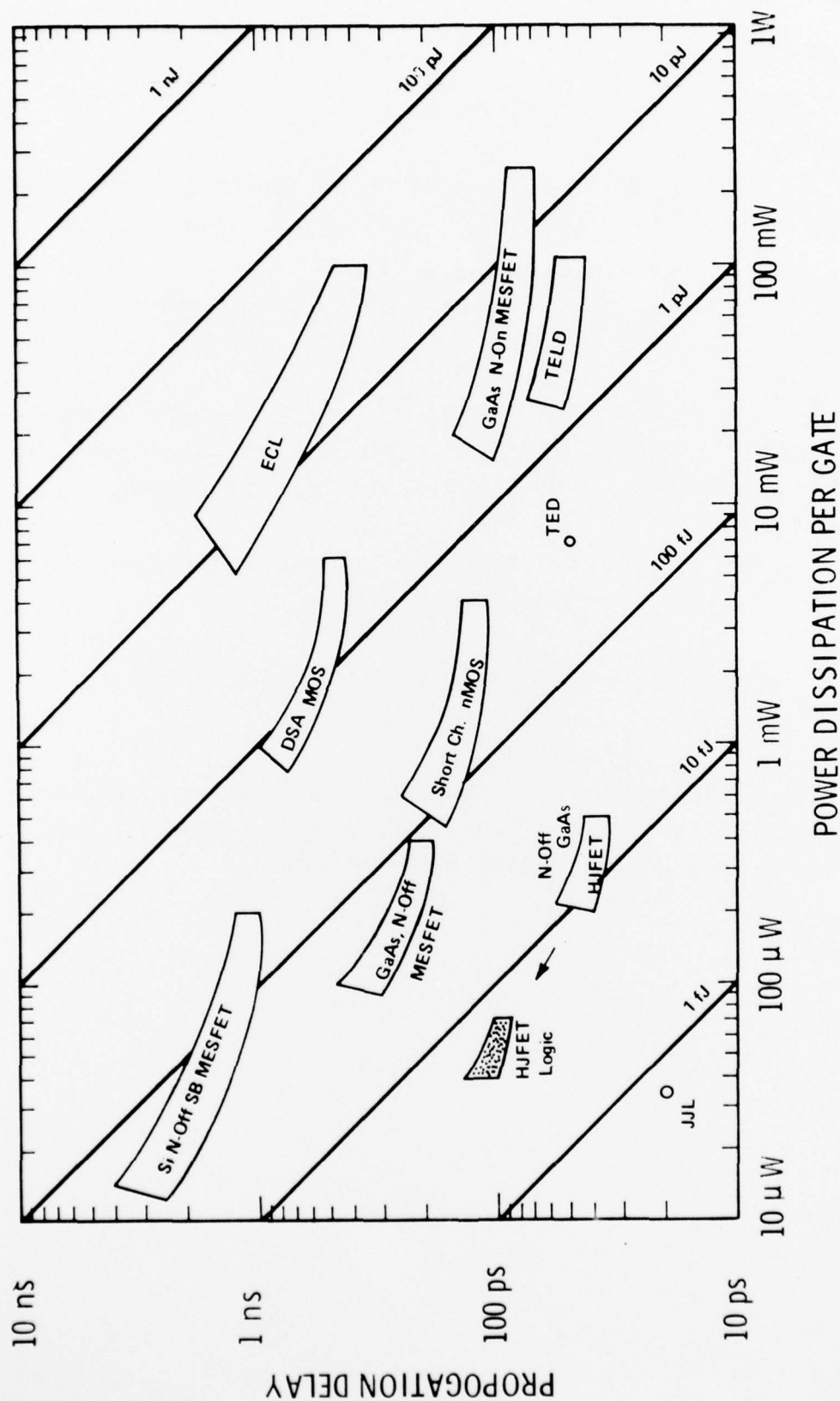


Fig. 40. Logic performance of GaAs-based high speed devices. The performance of the N-Off HJFET is that for an individual device. In a logic circuit however the delay time will be larger and could potentially be as little as about 150 ps.

4. REFERENCES

1. D. W. Shaw "Kinetics of Transport and Epitaxial Growth of GaAs with a Ga-AsCl₃ System," J. Cryst. Growth 8, 117 (1971).
2. S. M. Sze, Physics of Semiconductor Devices (Wiley-Interscience, New York, 1969).
3. R. Dingle, W. Wiegman, and C. H. Henry, "Quantum States of Confined Carriers in Very Thin Al_xGa_{1-x}As/GaAs/Al_xGa_{1-x}As Heterostructures," Phys. Rev. Lett. 33, 827 (1974).
4. R. L. Anderson, "Experiments on Ge/GaAs Heterojunctions", Solid State Electron. 5, 341 (1962).
5. L. J. Giacoletto (Michigan State University), private communication.
6. J. A. Turner and B. L. H. Wilson, "Implications of carrier velocity saturation in GaAs FET" in Intl. Symp. on GaAs, 1968, (IPPS, London, 1969) Paper No. 30.

APPENDIX

The dc drain saturation current (I_{DS}) of a FET in the saturation regime with a parallel depletion front is given by

$$I_{DS} = qN_D v_s \cdot (a-W) \cdot Z \quad , \quad (A.1)$$

where q is the electronic charge, N_D (10^{17} cm^{-3}) is the net donor concentration in the channel, v_s is the saturation electron velocity, W is the depletion depth, a is the active layer thickness, and Z is the channel periphery. The open channel current can be defined as

$$I_O = qN_D v_s Z a \quad . \quad (A.2)$$

Equation (A.1) can be written as

$$I_{DS} = I_O - qN_D v_s Z W \quad . \quad (A.3)$$

On the other hand, the depletion depth can be expressed as

$$W = \left[\frac{2\epsilon_o \epsilon_r}{qN_D \left(1 + \frac{N_D}{N_A}\right)} (V_{eff}) \right]^{1/2} \quad , \quad (A.4)$$

where ϵ_r is the relative dielectric constant of GaAs, ϵ_o the free space dielectric constant, N_A the net hole concentration of the gate semiconductor (10^{18} cm^{-3}), and V_{eff} the effective gate voltage causing the depletion. V_{eff} can be expressed as

$$V_{eff} = V_{bi} + E_M \cdot L_g + R_S I_{DS} - V_g \quad , \quad (A.5)$$

where kT/q is neglected and V_{bi} is the built-in potential of

heterogate junction (1.4 eV). E_M is the critical^{field}/(3.5 kV/cm for GaAs), L_g is the gate length, R_S is the source resistance, and V_g is the applied gate voltage (negative for N-ON and positive for N-OFF).

Substituting Eq. (A.5) into Eq. (A.4), one obtains

$$W = \left[\frac{2\epsilon_o \epsilon_r}{qN_D \left(1 + \frac{N_D}{N_A}\right)} (V_{bi} + R_S I_{DS} + E_M L_g - V_g) \right]^{1/2} \quad (A.6)$$

If Eqs. (A.3) and (A.6) are combined, the following is obtained:

$$I_{DS} = I_o - qN_D v_s Z \left[\frac{2\epsilon_o \epsilon_r}{qN_D \left(1 + \frac{N_D}{N_A}\right)} (V_{bi} + R_S I_{DS} + E_M L_g - V_g) \right]^{1/2} \quad (A.7)$$

The intrinsic dc transconductance g'_m is defined as

$$g'_m = \frac{\Delta I_{DS}}{\Delta V_g} \quad (A.8)$$

and so upon using Eqs. (A.6) through (A.8)

$$g'_m = \frac{\Delta I_{DS}}{\Delta V_g} = \frac{\Delta I_{DS}}{\Delta W} \cdot \frac{\Delta W}{\Delta V_g} = qN_D v_s Z \cdot \frac{1}{2W} \cdot \frac{2\epsilon_o \epsilon_r}{qN_D \left(1 + \frac{N_D}{N_A}\right)}$$

$$g'_m = \frac{v_s Z \epsilon_o \epsilon_r}{W \left(1 + \frac{N_D}{N_A}\right)} \quad .$$

Since $N_D/N_A = 0.1$, it can be neglected, so then

$$g'_m = \frac{v_s Z \epsilon_o \epsilon_r}{W}$$

and

$$v_s = \frac{g'_m W}{Z \epsilon_o \epsilon_r} \quad (A.9)$$

The extrinsic transconductance is given by

$$g_m = \frac{g_m'}{1 + R_s g_m'} \quad (\text{A.10})$$

so that measuring g_m and I_{DS} as a function of V_g and knowing the other parameters, one can calculate g_m' , W , and v_s in the channel.

Moreover, by differentiating Eq. (A.7) one finds that

$$\frac{\Delta I_{DS}}{\Delta \left[(V_{bi} + R_s I_{DS} + E_M L_g - V_g)^{1/2} \right]} = v_s 2Z \epsilon_o \epsilon_r \quad (\text{A.11})$$

Solving for v_s ,

$$v_s = \frac{1}{2Z \epsilon_o \epsilon_r} \cdot \frac{\Delta I_{DS}}{\Delta \left[(V_{eff})^{1/2} \right]}$$

is obtained. If I_{DS} in terms of the applied gate voltage is plotted as a function of $\sqrt{V_{eff}}$, the slope of this line can then be used to calculate v_s as a function of $\sqrt{V_{eff}}$ or W . Thus

$$v_s = \frac{\alpha}{2Z \epsilon_o \epsilon_r} \quad (\text{A.12})$$

where

$$\alpha = \frac{\Delta I_{DS}}{\Delta \sqrt{V_{eff}}} \quad .$$